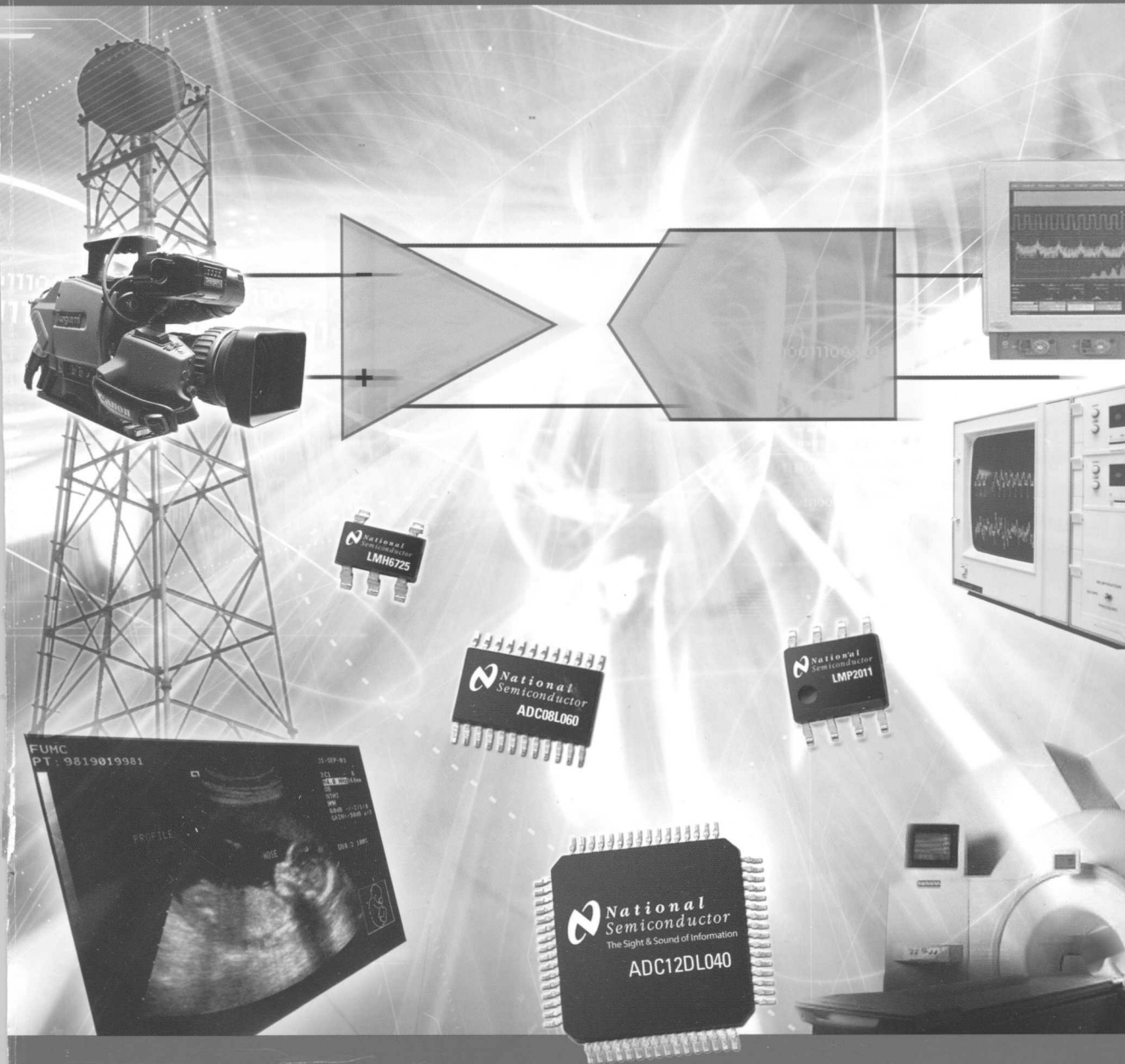


# Meeting Signal-Path Design Challenges

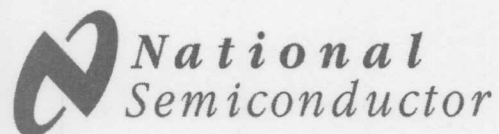
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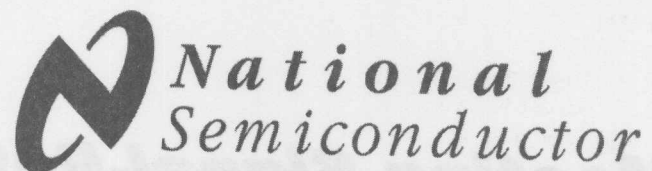


# ***Meeting Signal-Path Design Challenges***

**2005 Signal-Path Seminar**







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## ***Life at the Sharp End***

### **The start of the signal-path processing is... the Operational Amplifier**



7



Many signal paths start with that most universal of analog components, the operational amplifier\*. First named for its ability to perform mathematical operations (addition, subtraction, integration, differentiation etc) the modern Op-Amp provides the interface to many transducers and sensors, starting the process of converting real-world sensations such as sound, temperature, pressure, and light into electrical signals. Many signal sources simply require amplification or buffering, while others require manipulation to correct transducer or transmission errors. Op-Amps often can combine many of these functions, because the transfer characteristic of an Op-Amp is determined primarily by the external components connected around the Op-Amp.

Despite the fact that the Op-Amp is essentially a five-terminal device, with two input pins, two supply pins (or supply and ground), and one output pin, there are literally hundreds of Op-Amp types. National alone has more than 300 different types of Op-Amp, not counting duals, triples, and quads as separate types, and other manufacturers have similarly large portfolios.

During this seminar we will take a look at the characteristics that distinguish these Op-Amp types, why they are different, and how to choose the "right" Op-Amp. Techniques for solving common Op-Amp problems will be described, along with practical circuit applications.

The Op-Amp is only the first part of the signal path. Later on we will show how to accurately convert the signal to a digital format and then transfer that digital data, again without errors, to a storage or processing medium.

However, that is not where the signal path ends. Very often the signal information needs to be put back into a way that we in the "real world" can comprehend, either directly from the source or from the storage medium. Closing the circle, Op-Amps or their cousins are used to drive speakers, display devices, motors and RF transmitters.

\* A notable exception is RF receivers.







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2



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## What Is an Op-Amp?

- **Op-Amp stands for: operational amplifier**
  - Performs Mathematical “Operations” in the electrical domain
  - It is the building block of an analog computer: add/subtract, multiply/divide voltages and currents
- **Key properties of an Op-Amp**
  - Extremely high open loop voltage gain ( $>10^6$ )
  - High input impedance
  - Low output impedance
- **Used in hundreds of applications including**
  - Filtering
  - Level shifting
  - Buffering
  - Signal amplification



3



The name “operational” comes from the ability of the amplifier, with appropriate external connections, to perform mathematical *operations* such as addition, subtraction, multiplication, and division. More complex operations, such as integration and differentiation, are easily achieved.

By itself, an Op-Amp is pretty useless. Because of the large open-loop gain, any input signal, even just noise, is able to drive the output into the rails. But when you apply feedback, a part of the output signal is fed back to the input of the amplifier so that the amplitude of the output is now controlled by the feedback components.

This makes the Op-Amp general purpose: Different feedback networks can completely alter the total transfer characteristic of input signals to output signals. Closed-loop voltage gains ranging from  $-1000$  to  $+1000$  can easily be realized. Level shifting, signal inversion, and filtering can be accomplished and high impedance sensors can be buffered from low impedance loads.

Although these external feedback components are a significant factor in determining how the Op-Amp circuit performs, Op-Amps are not ideal. Each Op-Amp is tested for more than 30 parameters and some of these parameters are going to affect the overall performance in a given application far more than the rest. Some parameters can be improved (i.e. closer to ideal) only at the expense of others. Sacrificing DC precision for speed is an example. The technologies used to fabricate the Op-Amp will impact some parameters more than others.

## **Trade-offs in Op-Amp Specs**

- **One Op-Amp can't solve all application requirements**
  - **Bandwidth is a function of supply current**
  - **Noise performance is a function of die area and supply current**
  - **Process technology allows for optimization of certain key specifications dependent on application**
  - **Varied Op-Amp topologies also provide for optimization of certain key specifications**



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Some of the more fundamental trade-offs between Op-Amp parameters are shown here. If higher speed or lower noise is important, then the supply current drawn by the amplifier goes up. This will have a strong impact where the power supply is a battery and long operating life is required. Also with a battery, the negative rail is usually ground and the input stage must be designed to take this into account. To get the best overall performance for a group of parameters sometimes the process technology becomes the dominant factor. For example, BIPOLAR processes are popular for applications requiring low voltage noise, high speed, or the capability to drive heavy loads. CMOS processes are useful for applications with low supply voltages where output dynamic range is important or when high impedance sources are anticipated. BiCMOS processes help provide a combination of input/output requirements.

Most catalogs will present available Op-Amps in broad categories with similar key parameters.

## Typical Op-Amp Categories

- **Audio (Power):** THD, power bandwidth, continuous output power
- **Audio (Pre-Amp):** THD, noise, frequency response, slew rate
- **High power (DC):** Supply voltage, output current, saturation voltage



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Although every amplifier will be subjected to similar tests, only a few of those tests will be considered critical for a given application. Leaving out supply voltage and supply current ratings, there may be only three or four other specifications that determine whether the Op-Amp is suitable.

For example in audio, frequency response beyond 20 kHz with THD values as low as 0.001% may be required. Although the input signal maximum slew rate is realistically less than 0.5 V/\_s amplifiers will tend to have slew rates 10 to 20 times greater than this to get that low distortion. General purpose Op-Amps have noise voltages over 50 nV/\_Hz. For high quality audio, something under 5 nV/\_Hz is needed.

If the application is driving a small motor, then the ability of the output to swing close to the voltage rails is important for delivering the maximum power, and the output current must be sufficient for the size of the load.



## Op-Amp Categories

- **High-speed (small signal):**  $f_{-3dB}$ , GBW
- **Video:** Differential gain,  
Differential phase,  $I_{OUT}$
- **High-speed (large signal):** Slew rate,  
Settling time
- **Precision:**  $V_{OS}$ , gain,  $1/f$  noise



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For high speed, a wide closed-loop bandwidth compared to the input signal frequency range is needed. Because most applications are AC coupled, the DC specifications, such as offset voltage and drift, are not nearly as important. Even in video, where the signal is DC coupled, the relatively low gains used rarely make offset voltages important, but the common mode performance is important. Therefore in video applications, there are two extra specifications, differential gain and differential phase, which are not commonly found on other Op-Amp datasheets.

In ATE the ability to change DC levels rapidly is important to minimize test times, and the slew rate and time to settle to the final value are important.

In precision applications, many sensors generate low-amplitude signals at relatively low frequencies, including DC. Specifications to watch for are offset voltages and the changes with temperature, supply voltage, and time. Low frequency noise is particularly troublesome. With few exceptions, the noise voltage of an Op-Amp increases from the broadband value as the frequency approaches DC and has a  $1/f$  characteristic. Although not always specified (other than as a typical value), the corner frequency at which the noise begins to increase is an important parameter for a precision Op-Amp.

## Op-Amp Categories

- **Low voltage/low power:**  
Supply voltage range,  
Supply current maximum  
Output voltage swing at  
specified load current
- **Single-supply:**  
Input common-mode to supply or  
ground rail  
Output rail-to-rail



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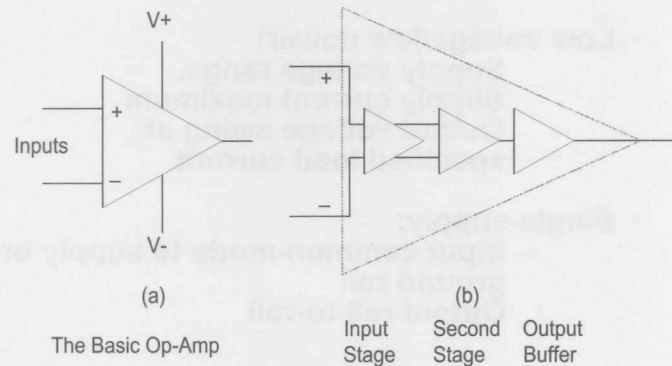
Low voltage and low power are usually taken to be synonymous. Designed to operate from battery power sources, these Op-Amps are expected to have low operating supply currents to minimize battery drain. As noted earlier, the reduced supply currents mean that this class of Op-Amp is not going to have high bandwidths or high slew rates. Supply currents run from as low as 50  $\mu$ A to as high as 1.5 mA with corresponding GBW products from 50 kHz to 3 MHz.

For low voltage applications, the operating supply voltage is a key parameter, and many Op-Amps will operate on a 2.7 V or lower supply. Some amplifiers will work as low as 0.9 V, but are not always specified at that voltage. Because of the reduced dynamic range offered by low supply voltages, rail-to-rail outputs are often offered. There is no industry definition of what a rail-to-rail output is, but it is generally accepted that the output must swing to less than 700 mV from the supply rail. With light loads, many amplifiers can swing to within less than 10 mV of the rail.

Many of the Op-Amps in this category are also called *single-supply* Op-Amps, which, apart from having a wide output dynamic range, means that they also have input stages capable of being biased at one of the supply rails, typically ground. This enables the signal to swing a few hundred millivolts below ground without affecting the performance.

It is normally less important for the input common-mode range to include both the supply rails but Op-Amps that can do this are referred to as RRI/O amplifiers. Certain applications, such as automotive, may require the input common mode range to exceed either or both supply rails by wide margins (many volts).

## The "Classic" Op-Amp



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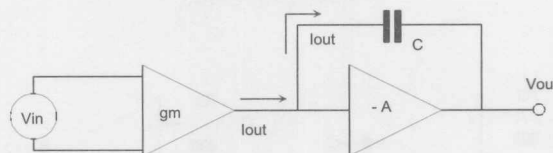
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As noted earlier, all Op-Amps are pretty much the same with two inputs, two supply pins, and one output. Early Op-Amps may have had additional pins for external frequency compensation and even ground pins, but most operated on split supplies to allow signal inputs at ground potential. When the negative supply pin is tied to ground, the non-inverting input is DC biased to halfway between ground and the positive supply rail. Later we will look at input stages that allow the input signal common-mode voltage to be at ground potential even when there is no negative supply rail.

Internally the classic Op Amp has three stages; a differential input stage, a gain stage, and an output single-ended buffer stage. Over the years (starting from the uA702 of 1964) there have been many different ways of implementing these three stages, and these have contributed directly to the differences between Op-Amps. Interestingly, there has been only one major change to the basic topology and that was with the introduction of current feedback (CFB) integrated Op-Amps in the 80s.

## AC Gain Model (Open Loop)



$$i_{OUT} = gm \times v_{IN}$$

$$v_{OUT} = i_{OUT} / 2\pi f C$$

$$v_{OUT} / v_{IN} = gm / 2\pi f C$$



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The input stage of an voltage feedback (VFB) Op-Amp is modeled as a transconductance stage in which the small differential input voltage is converted into a current that drives the second stage. The second stage is shown as a high-gain inverting amplifier with a frequency compensation capacitor connected across the input to output. This compensation is necessary to prevent the amplifier oscillating at high frequencies when external feedback is applied.

In the absence of feedback components, the open loop amplitude response exhibits a low frequency pole determined by the size of the compensation capacitor, and a steady roll off in gain towards unity gain at some high frequency  $f_U$ .

This simple model makes it very easy to calculate the open-loop AC gain  $A(f)$  of the Op-Amp at any frequency  $f$ .

Since the first stage is a transconductance stage ( $gm$ ), then the input voltage  $v_{IN}$  is converted to an output current  $i_{OUT}$

$$i_{OUT} = gm \times v_{IN}$$

This current flows through the capacitor  $C$  to produce the output voltage  $v_{OUT}$

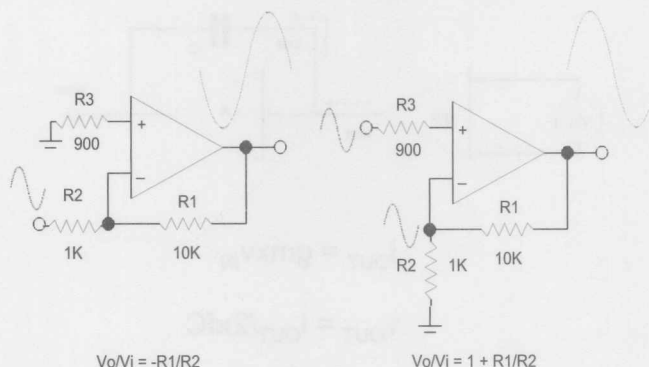
$$v_{OUT} = i_{OUT} \times 1 / 2\pi f C$$

Substituting for  $i_{OUT}$  and rearranging, we get

$$v_{OUT} / v_{IN} = A(f) = gm / 2\pi f C$$

This final equation shows that the frequency response of an ideal VFB Op-Amp is identical to that of an RC low-pass filter. This means that at mid to high frequencies there will be a  $90^\circ$  phase shift between the non-inverting input and the output of the Op-Amp. Op-Amps are not ideal, and additional phase shifts caused by the internal active and passive components means that the total phase shift can exceed  $90^\circ$  and reach  $180^\circ$  at some frequency. With feedback to the inverting input, if the amplifier loop gain is greater than unity when this happens, the Op-Amp will oscillate.

## Closing the Loop (VFB)



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For most applications, closing the feedback loop means that the response of the Op-Amp is determined by the value of the external components rather than the precise characteristics of the Op-Amp itself. This leads to a very intuitive analysis of the way an Op-Amp works, which is valuable because it provides a basis for the need to evaluate the impact of second or third order effects. A designer can therefore choose whether or not to spend time on a more complex analysis.

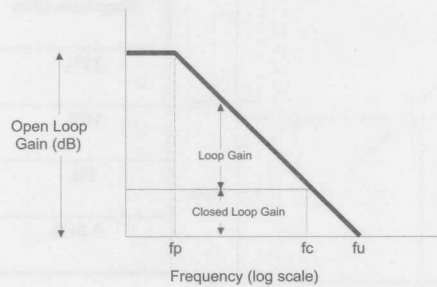
**For a VFB amplifier it is assumed that no signal current flows either into or out of the input pins and that the voltage on each input pin is identical to the other (as the result of negative feedback from the output to the inverting input).**

For the inverting amplifier above, the non-inverting input is connected to ground through a resistor. This means that the non-inverting input voltage will *always* be 0 volts. When a signal, possibly several volts in amplitude, is applied to the resistor R2 connected to the inverting input, feedback from the output through the resistor R1 will keep the inverting input also at 0 volts. Since the input pin current is zero, any current produced by the voltage difference across R2 must flow in R1. With the resistor values shown above a 1 V input produces a 100  $\mu$ A current in R2. This same current flowing in R1 means the output voltage is -10 V, for a closed-loop gain of -10. The gain is simply  $-R_1/R_2$ . Because the inverting input is constrained to 0 V it is said to be at a *virtual ground*. It actually doesn't have to be 0 V. If the non-inverting input was tied to  $V+/2$ , then the output would hold the inverting input to  $V+/2$ .

For the non-inverting amplifier, feedback will make the inverting input track the non-inverting input. If the non-inverting input changes by 1 V then the inverting input will change by 1 V. For this to happen, the output has to change by 11 V and the gain is  $(1 + R_1/R_2)$ .

Note that the analysis takes advantage of the fact that the two inputs are always held to the same voltage. Even if reactive feedback components are used, this is still true. When the inputs are at different voltages, the amplifier is open loop and there are likely to be problems. We will discuss this later on.

## VFB Closed-Loop Response



$$f_c = f_u / (1 + R_1/R_2)$$



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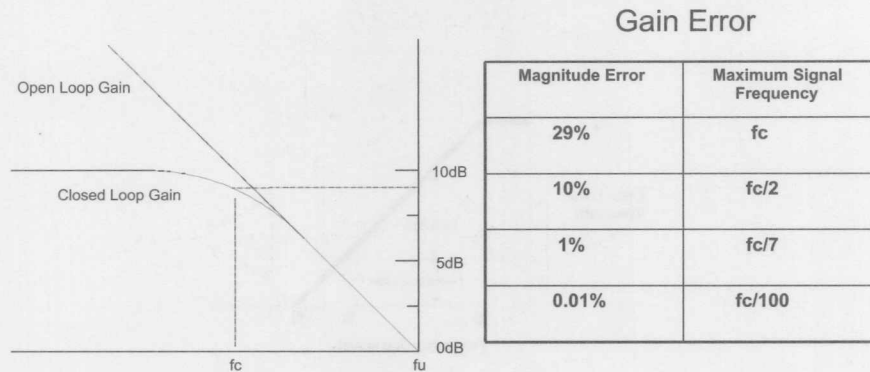
In the intuitive analysis no reference is made to signal frequency but, as shown previously, the Op-Amp open-loop response is similar to that of a low pass RC filter. What does this mean for the closed-loop response? Using feedback theory to derive the closed-loop relationship between the input voltage and the output voltage, taking into account the frequency dependency introduced by the compensation capacitor, it can be shown that the upper -3 dB frequency corner of the closed-loop response,  $f_c$ , is related to the open-loop 0 dB gain frequency,  $f_u$ , and the feedback factor (the fraction of the output that is fed back to the input) such that

$$f_c = f_u / (1 + R_1/R_2)$$

The most obvious consequence of this relationship is that as the closed-loop gain is increased the closed-loop bandwidth decreases. Less obvious is the impact this will have on stability and signal fidelity.



## High Frequency Performance



For an  $\frac{1}{2}$  LSB error (12-bit) at 10 kHz (0.125%) and a gain of 20,  $f_c = 2$  MHz and  $f_u = 20$  MHz



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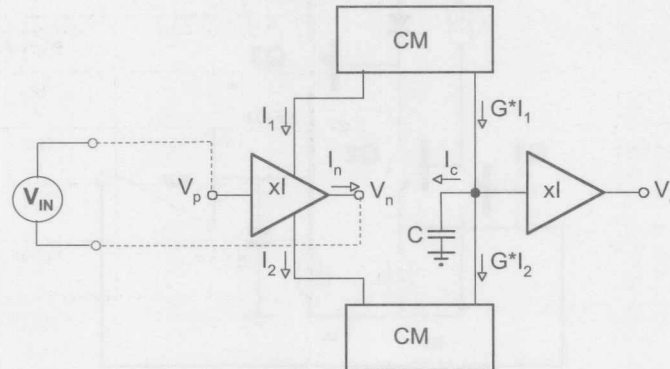


Op-Amps are available with bandwidths quoted from a few hundred kilohertz to several hundred megahertz, and since many applications utilize signal frequencies from DC to a few thousand hertz it would seem that a constant gain bandwidth product is not going to be especially limiting. Even so care should be taken when it comes to choosing the right Op amp. Continuing the parallel with the RC low pass filter, the Op-Amp closed-loop frequency response needs to be much higher than the maximum signal frequency. At the upper cut-off frequency,  $f_u$ , the gain will be -3 dB compared to the gain at low frequencies. This is a 29.3% error. If the highest signal frequency is 0.1  $f_u$ , the gain error is -0.04 dB which is 0.5%. This may not seem to be much of an error, but it is the *entire* error budget in a 7-bit system. For a half LSB error in a 12-bit system (0.125%) the gain error should be less than 0.011 dB, which corresponds to a maximum signal frequency of 0.05  $f_u$ ! For a 10 kHz signal at a gain of 20, this requires a 2 MHz closed-loop bandwidth – and an open-loop bandwidth of over 20 MHz.

Any design with a VFB Op-Amp has to take into account that the closed-loop bandwidth at the desired closed-loop gain may effect the overall desired performance. Stated another way, the amplifier closed-loop bandwidth at the desired gain has to be large enough not to limit the gain over the signal bandwidth.

The same restrictions on gain accuracy versus closed-loop bandwidth on the VFB Op-Amp hold true for a current feed back (CFB) Op-Amp but, unlike the VFB Op-Amp, the CFB Op-Amp can maintain the same closed-loop bandwidth as the closed-loop gain is increased.

## Current Feedback (CFB) Op-Amp Open-Loop Model



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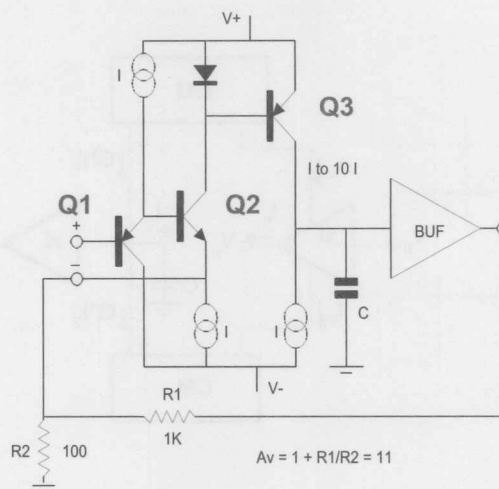
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Just like the classical VFB Op-Amp, the CFB Op-Amp is comprised of three stages, but two of these stages are significantly different. Instead of an input transconductance ( $g_m$ ) stage, the input stage of a CFB Op-Amp is simply a unity gain voltage buffer. As far as the source signal is concerned, the non-inverting input is high impedance (just like a VFB Op-Amp), but the inverting input is low impedance (the output of a voltage follower). From the application viewpoint this immediately limits the use of the Op-Amp for inverting circuit designs. The second stage (the current mirrors CM) uses the current flowing in the input stage to provide current gain to the output stage, which is a voltage follower similar to that used in the VFB Op-Amp. The capacitor C compensates the Op-Amp (just as in the case of the VFB Op-Amp) but this a significantly smaller capacitor,  $<1$  pF, than that used by a VFB Op-Amp.

When we apply feedback, unlike the VFB Op-Amp, the effect will be to ensure that the input stage currents ( $I_1$  and  $I_2$ ) are the same.

**For a CFB Op-Amp, it is assumed that the input stage inverting and non-inverting currents remain the same (as the result of feedback from the output to the inverting input).**

## Current Feedback (CFB) Op-Amps



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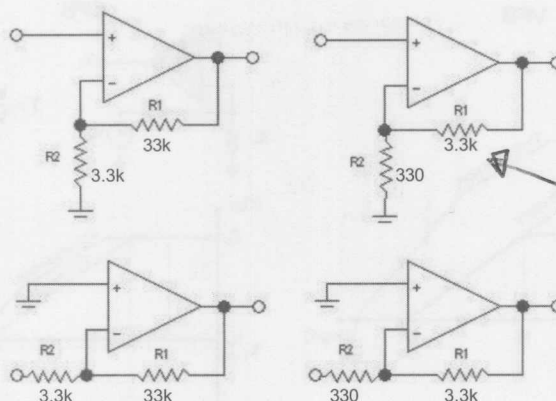
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This is a much simplified schematic where Q1, Q2, and Q3 handle positive input voltage swings. Most CFB Op-Amps will have a similar stage connected to the negative rail which will mirror the operation of Q1, Q2, and Q3 for negative signal swings. Both inputs are constrained to be at the same voltage (neglecting the slight difference in  $V_{BE}$  between PNP and NPN transistors) so the effect of feedback from the amplifier output is **not** going to be maintaining the differential voltage as close to zero as possible. Instead, the inverting input is going to track any voltage changes in the non-inverting input because the input stage is essentially a voltage follower.

To understand how the circuit works, assume that the non-inverting input is initially at ground potential or 0 V. Going up a diode drop and down a diode drop means that the inverting input is also at 0 V (near enough), and no current flows in R2. Now raise the non-inverting input by 1 V. The inverting input goes up by 1 V and 10 mA flows in R1. Without feedback the current in Q2 has to increase by 10 mA. Of course, the same 1 V increase in the non-inverting input voltage is multiplied by the amplifier gain (many thousands of times) to the output stage. This means that the output voltage increases until it is able to deliver 10 mA through R1 to satisfy the current demand in R2, at which point the current in Q2 is restored to its original quiescent value. Therefore the output rises to 11 V when the input rises 1 V for a closed-loop gain of  $1 + R1/R2 = 11$ . The effect of feedback has been to restore the same current levels flowing in the input transistors that existed before there was a change in the non-inverting input. Rather than making the input stage voltages the same, CFB works to make the currents the same.

Note that the closed-loop gain is given by the ratio of the external feedback resistors and is identical (at DC and low frequencies) to that obtained for a VFB Op-Amp.

## VFB & CFB Op-Amp Closed-Loop Gain



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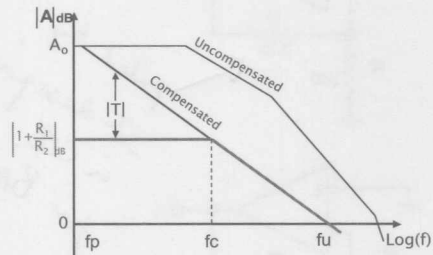
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At first glance, despite the difference in the action of the feedback loop, it appears there is no real difference in the external components used for either type of Op-Amp. In each case, the gain is set by the resistor ratios. However, note that in the case of the CFB Op-Amp, the resistor values are much lower than those of the VFB Op-Amp. For a non-inverting amplifier, this may not mean much, but for an inverting amplifier the small value of R1 can cause significant loading on the source. The difference in impedance levels can be traced back to the open loop characteristic of the CFB Op-Amp.

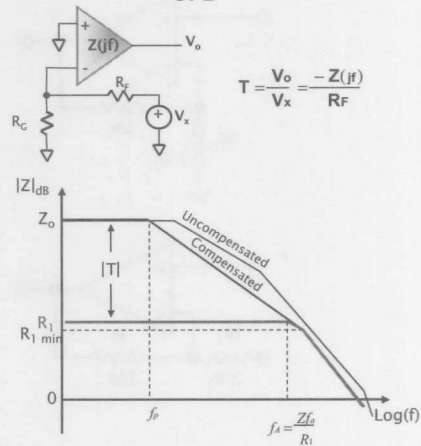
*for Inverting  
don't use CFB.*

## VFB & CFB Op-Amp Loop Characteristics

VFB



CFB



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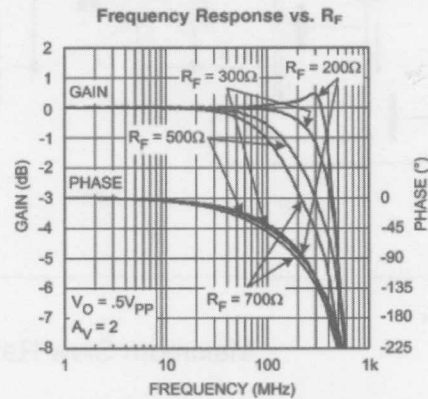
16

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Again, at first glance, the open- and closed-loop curves for a VFB and a CFB Op-Amp are very similar, except for the important point that the Y axis for the VFB Op-Amp is open-loop voltage gain (a dimensionless number), and that for the CFB Op-Amp is open-loop forward transimpedance. When the loop is closed, the bandwidth of the VFB Op-amp is set by the ratio of the feedback resistors R1 and R2. For the CFB Op-Amp it is set by the value of R1. This means that for a given CFB Op-Amp, the Op-Amp designer chooses the size of the feedback resistor R1 to achieve the design closed-loop bandwidth. Put another way, for a given CFB Op-Amp bandwidth, the size of R1 is pre-determined. As we will see on the next page, the user has the option of changing R1 over a limited range to tailor the frequency response characteristic of the CFB Op-Amp.

## Changing the Value of R1 ( $R_F$ )

### (LMH6715) Control over Bandwidth with Feedback Resistor



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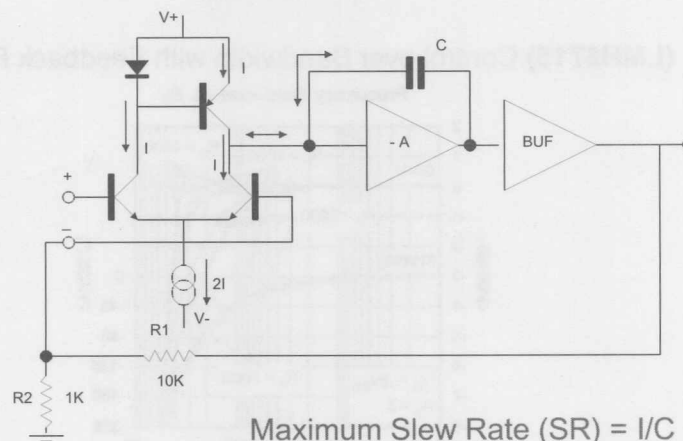
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Because  $R_1$  has such a large effect on the CFB Op Amp, in general the user is recommended to keep to the values shown on the datasheet. Some tailoring of the frequency response is possible by adjusting the value of  $R_1$ . For the LMH6715 shown here, the gain is fixed at +2 and the amplitude and phase are plotted for a range of values for  $R_1$ . Higher values for  $R_1$  result in lower bandwidths, but a flatter amplitude response through that bandwidth. Correspondingly, lower values for  $R_1$  can produce much wider bandwidths at the expense of some peaking in the amplitude response.



## Slew Rate Limit



$$\text{Maximum Slew Rate (SR)} = I/C$$

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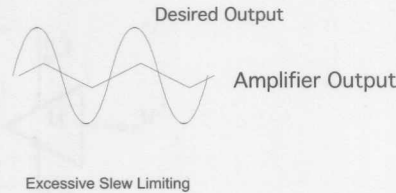
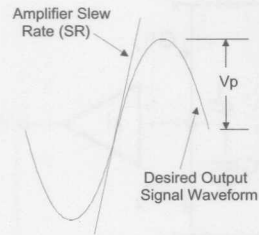
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The schematic above is still much simplified compared to modern Op-Amps but nevertheless shows the mechanism involved in *large-signal* operation of the Op-Amp. Under normal closed loop operation, feedback from the output forces the inverting and non-inverting inputs to the same voltage (VFB). This should be self evident since with a high amplifier gain ( $>100,000$ ), a 1 mV differential input would drive the output to 100 V! Therefore under normal conditions, the input voltages are within a few microvolts of each other regardless of the amplitude of the input signal. Under balanced conditions, the input transistors share the tail current equally, and no net current flows to charge or discharge the capacitor. When one input changes relative to the other, current will flow in the capacitor and the amplifier output voltage moves to bring the inputs back into balance. Now assume that one input is changing very rapidly, requiring the capacitor to charge or discharge at a very high rate. The maximum current  $I$  available to the capacitor  $C$  is the tail current and this, along with the size of the capacitor, will determine how fast the output can *slew* or change along with the signal.

$$\text{Slew rate} = I/C$$

For a general purpose amplifier with  $I=20 \mu A$  and  $C=30 \text{ pF}$ , the slew rate is  $0.67 \text{ V}/\mu s$ . High-speed Op-Amps are capable of slew rates in excess of  $4,000 \text{ V}/\mu s$  and how these rates are achieved will be discussed later. The important thing to recognize is that when the slew rate limit is reached, the output cannot change fast enough for the feedback loop to keep the input differential stage in balance. The input differential signal is no longer small and the amplifier is open loop. Distortion will go up (even before the slew rate limit is reached) and this may have a significant impact on the application.

## Slew Rate & Bandwidth



$$V_o = V_p \sin 2\pi f t$$

$$dV_o/dt = 2\pi f V_p \cos 2\pi f t$$

$$= 2\pi f V_p \text{ (at } t = 0 \text{)}$$

$$SR = 2\pi f_{\max} V_p$$

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Even if we neglect the amplitude error that occurs as the signal frequency approaches  $f_u$ , it is important to remember that this is the small signal bandwidth. As a sine wave signal increases in amplitude so does the slope of the waveform increase at the zero crossing point. If this slope increases to the point that the amplifier output cannot follow the slope, the amplifier slew rate has been exceeded, and then the output will tend toward a triangular wave rather than a sine wave.

Even before the slew rate limit is reached, distortion will have increased since the differential voltage at the Op-Amp inputs is getting larger than a few microvolts in order to provide the increase in slewing current demanded by the compensation capacitor. Therefore, the full power bandwidth is going to be less than the small signal 3 dB bandwidth  $f_u$ .

The maximum full power signal frequency,  $f_{\max}$ , is given by

$$f_{\max} = SR/2\pi V_p$$

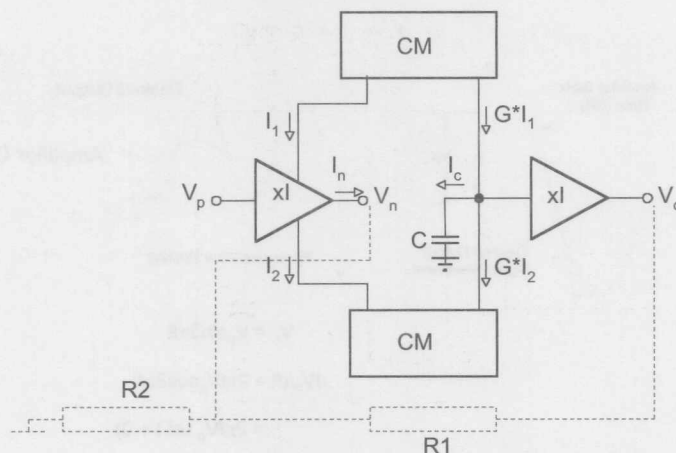
where SR is the slew rate and  $V_p$  is the peak signal voltage. Take the example of a fast Op Amp, the 200 MHz LMH6672, being used as a 2X gain amplifier with an output signal level of 2 V(p-p). At a gain of 2, the small signal closed-loop bandwidth is 100 MHz. The slew rate is 170 V/ $\mu$ S so the full power bandwidth is only  $170/2\pi = 27$  MHz.

To get a realistic full power bandwidth of up to 100 MHz the slew rate has to be increased by a factor of at least five, since distortion will have started to increase before the full power bandwidth frequency is reached. A good choice would be the LMH6682 which is a 190 MHz amplifier with a slew rate of 940 V/ $\mu$ s.

To increase the slew rate of VFB Op Amps, the input stage has to be modified in order to provide more slewing current for the compensation capacitor under large signal conditions.

*slew Rate > 10, max updt slew rate  
for low distortion  
on Vfb.*

## CFB Op-Amp Slew Rate Limit



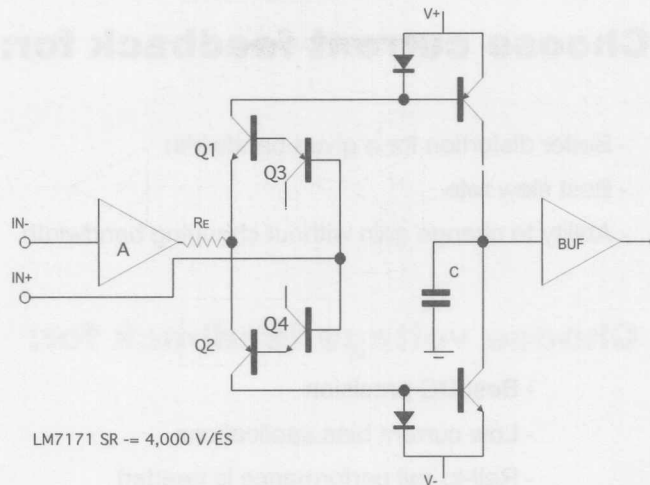
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In the case of the CFB Op-Amp, if the output voltage cannot move fast enough to provide the current in R2 produced by the input voltage change, this current will flow in the input stage. This input current, multiplied by the gain of the current mirrors, is available to charge or discharge the much smaller compensation capacitor C. The CFB Op-Amp will have a very high slew rate.

This does not mean that the CFB slew rate will always exceed that of a VFB Op-Amp.

## Enhanced Slew Rates



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The LM7171 is a good example of how the slew rate of a VFB Op-Amp can be increased, in this instance to over 4,000 V/μS!

Transistors Q1 through Q4 form the equivalent CFB Op-Amp input buffer with  $R_E$  being the equivalent of the feedback resistor. The inverting input is buffered by stage A, and the current available to charge or discharge the compensation capacitor is the differential input voltage divided by  $R_E$ .

## **CFB or VFB?**

### **Choose current feedback for:**

- Better distortion for a given bandwidth
- Best slew rate
- Ability to change gain without changing bandwidth

### **Choose voltage feedback for:**

- Best DC precision
- Low current bias applications
- Rail-to-rail performance is needed



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One consequence of the CFB topology is that the size of the resistor R1 connected from the output back to the inverting input will determine the closed-loop frequency response. The first thing to notice is that this is a relatively low valued resistor, generally less than 3 k $\Omega$ . Therefore, the resistor R2 will be even smaller for any reasonable values of closed loop gains. Many inverting applications require that the amplifier input does not load the source, so CFB Op-Amps are less suitable than an equivalent VFB Op-Amp. Since R1 sets the bandwidth, reactive components in the feedback path should be avoided since they can easily cause instability. Because the input stage is essentially unbalanced, the CFB Op-Amp is not well suited to precision applications. In the non-inverting mode the CFB Op-Amp excels at high speed, providing flat frequency response over wide bandwidths and with lower distortion at higher frequencies. The intrinsically high slew rates are useful in applications where the load voltage must change as rapidly as possible (pin drivers in ATE).

VFB Op-Amps suffer from the limitation in closed-loop bandwidth as the closed loop gain is increased. At high frequencies they are less able to maintain gain flatness compared to the CFB Op-Amp. Typically they exhibit much lower slew rates. On the other hand, they are more versatile, operating in many inverting applications denied to a CFB Op-Amp. The balanced input stage makes achieving precision easier and many VFB Op-Amps are available with rail-to-rail inputs and outputs.

The incredible variety of Op-Amps means that there is substantial overlap in performance characteristics. The challenge is to choose the Op-Amp for the features needed by the application, and not paying for features that may be intrinsic to the topology, but not needed by the application.

## Low Voltage, Low Power

- Single supply  $5\text{ V} \leq V_{+} \leq 2.7\text{ V}$
- Low current  $1\text{ mA} \leq I_Q \leq 10\text{ }\mu\text{A}$
- Rail-to-rail output Rail  $\pm 100\text{ mV}$
- Beyond the rail input



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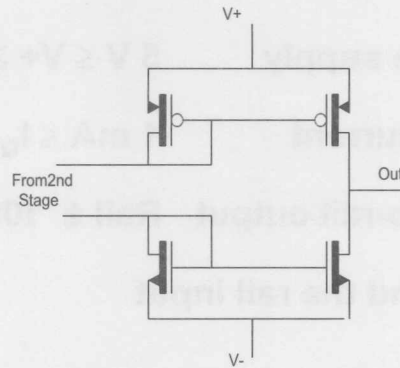
In an era of personal electronics, many signal-path applications are relatively low-frequency (slow) and are powered by batteries and has resulted in a class of Op-Amps known as “Low Power” Op-Amps. Early members of this class were built on CMOS processes, leading many people to think that CMOS consumes less power than Bipolar and is therefore the logical choice. In fact CMOS is low power when used in a digital application where the transistors are either on (1) or off (0). When used in a linear application, the CMOS transistor needs 40 times the current of a bipolar transistor for the same transconductance! The real reason CMOS was chosen is that when the supply voltage is reduced, the output dynamic range is reduced correspondingly. For many Op-Amps the output cannot swing close to the rails. The Class AB output stage (a common emitter configuration) saturates at least 0.9 V from the rail (or as much as 9 V from the rail for a power audio amplifier). On a 2.7 V supply this would limit the output swing to less than 0.9 V(p-p). To qualify as a rail-to-rail output the output voltage should swing to less than 100 mV from the supply rail. The output swing of a CMOS common source Class AB output stage is limited by the  $RDS_{ON}$  of the transistors and the load current. With light loads, the output can swing to less than 10 mV of the rail.

Similarly on the input side, it is important that the source can be biased close to one of the rails (usually the negative or ground rail) and have the amplifier perform as advertised. In fact most of these *single supply* Op-Amps can operate with a source biased as much as 300 mV beyond the rail.

With low supply currents the bandwidth and slew rate will be less than expected. Typically, a 1 mA amplifier will have a GBW of 1-3 MHz and a slew rate around 1 V/ $\mu$ s. If the current drops to 100  $\mu$ A, the bandwidth will be less than 50 kHz and the slew rate will be less than 0.1 V/ $\mu$ S. If the bias current in the output stage is very low, then even a small capacitive load (a ‘scope probe) can trigger oscillations.

Careful evaluation of the claims made on the front page of the datasheet is recommended!

## The CMOS Output Stage



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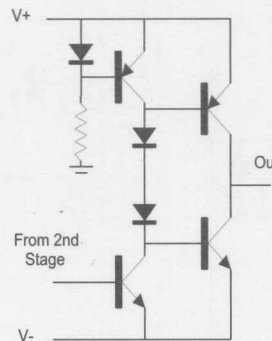
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The availability of complementary P and N channel transistors in a CMOS process has made this the technology of choice when it comes to rail-to-rail outputs. With a common source Class B or AB output stage the output can swing to a saturation voltage drop of either rail. This voltage drop is dependent on the load current and the  $R_{DS(on)}$  of the MOS device and, for light loads, can be just a few millivolts. One thing to remember is that with a common source connection, the output stage is no longer a voltage follower. Instead, it will have voltage gain depending on the size of the load resistor. With high resistance loads (25 Kohm to 50 Kohm) the output can swing very close to the rail because of the light load currents (less than 200  $\mu A$  on a 5 V supply) and the open-loop gain will be high due to the output stage gain. With a 600 Ohm, load the open-loop gain will be lower and the output will not swing as close to the rail.

*On rail to rail output,  
output load affects open loop gain  
- affect performance*

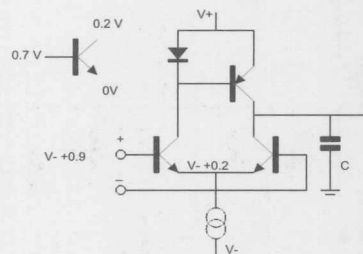
## Bipolar Output Stage



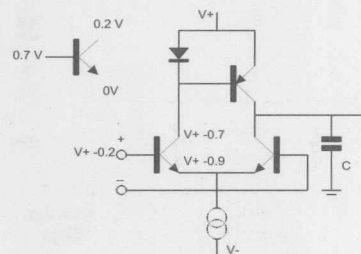
A bipolar output can also be connected in a common collector configuration to maximize the output swing but now the swing to rail is limited by the transistor collector saturation voltage rather than the load current. This will be around 100 mV to 200 mV. Bipolar output stages can deliver more current than their CMOS counterparts and will have wider bandwidth for driving large signals.



## Input Stage Design



(a) Negative swing



(b) Positive swing



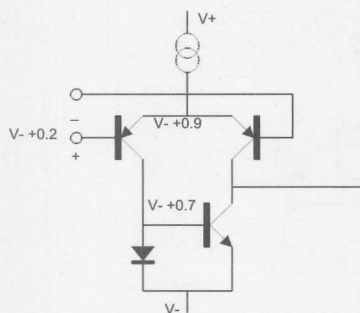
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As with the bipolar output stage, it is the saturation voltage and diode voltages of the transistors that determine how close the input signal can swing to the supply rail. For a negative swing, 0.7 V will be lost across the input base-emitter diode with a further 0.2 V across the tail-current source. This limits the negative swing to 0.9 V above the negative rail.

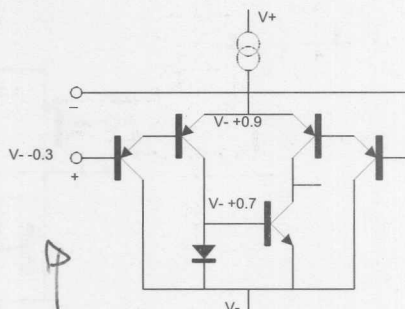
On the positive swing side, 0.7 V is lost across the diode in the current mirror and a further 0.2 V collector to emitter saturation voltage. This put the emitter at 0.9 V below the positive rail, so the base can swing  $0.9 \text{ V} - 0.7 \text{ V} = 0.2 \text{ V}$  from the positive rail. More complex circuits may limit the swing even more. If PNP input transistors are used, the swing limits to the positive and negative rails are reversed.

## Swinging to the Negative Rail



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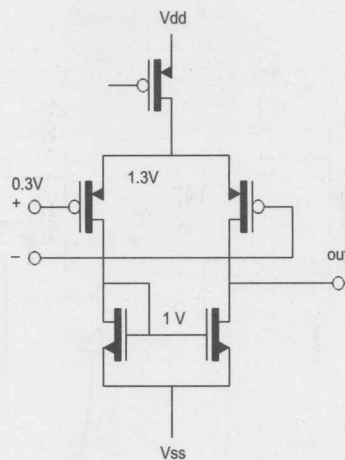
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With a PNP input stage, the signal can swing to within 200 mV of the negative rail. Actually, it is easy to see how the input can be made to swing *below* the negative rail by adding a second PNP to each input (a Darlington configuration). This second transistor adds another -0.7 volts so that the input can go 300 mV below the negative rail. For the NPN stage, a similar Darlington configuration will allow an input swing above the positive rail.

## CMOS Input Stage



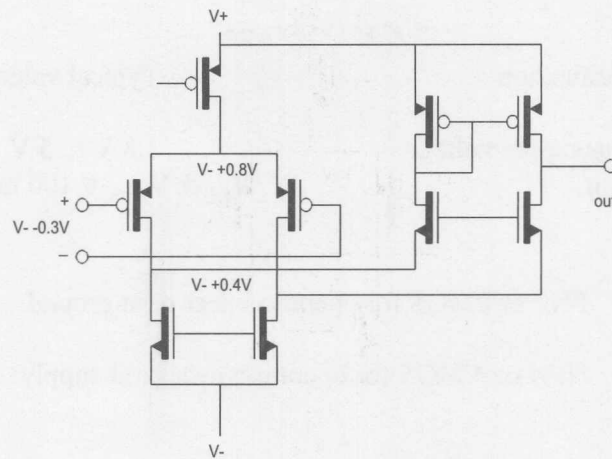
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A similar analysis can be made for the CMOS input stage. With a  $V_{gs}$  voltage of 1 V a P channel input can accommodate input signal swings to within about 300 mV of the negative rail. The prime limitation here is the voltage required across the lower current mirror.

## The Folded Cascode



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If the current mirror is replaced with a folded cascode stage then the inputs can extend 300 mV below the negative rail. This method of turning the signal around compared to a current mirror has the additional benefit of providing signal gain.

## To-the-Rail Inputs

### Key specification

### Typical values

Operating supply voltage

1.8 V to 5 V

RR output

$V_{IN} \text{ \& } V_{OUT} \leq 100 \text{ mV of Rails}$

PNP or PMOS for operation near or at ground

NPN or NMOS for operation near or at supply

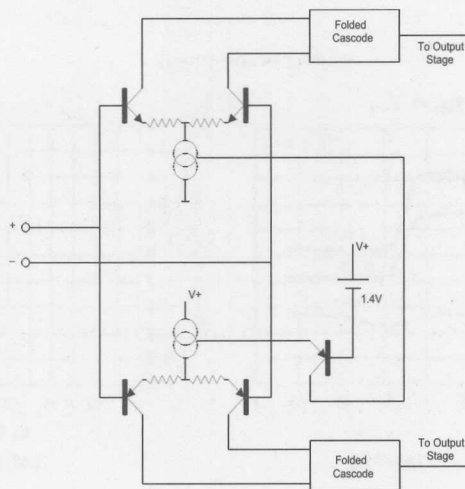


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For a low-voltage Op-Amp, the input stage can be either PNP or PMOS if operation at the negative rail is needed, or NPN or NMOS for operation at the positive rail. These classes of Op-Amps are also known as single supply Op-Amps.

## Rail-To-Rail Inputs



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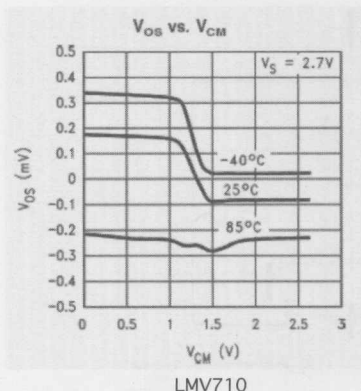
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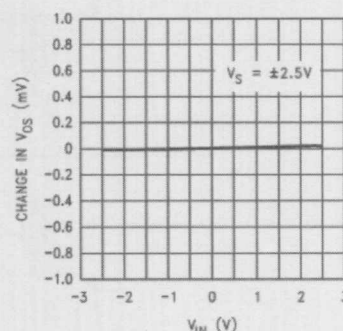
When operation at both input rails is required, a tandem input stage of two differential pairs is used. When the input common-mode voltage is close to the positive rail, the upper NPN pair will be processing the signal. When the common-mode input voltage is about 1.5V below the positive rail conduction transfers to the PNP pair and stays there as the negative rail is approached. The reason that the transition voltage is close to the positive rail is that most applications are biased at half supply or less and, under normal input conditions, the signal will not pass through the transition region. When it does pass through the transition region, there will be a change in the offset voltage and the input bias currents will reverse. For low distortion, it is best to avoid operating through the transition region.

It is worth noting that if operation near either rail is required, a single supply Op-Amp is probably the best choice. Inverting applications do not have any common swing on the input, and only a non inverting unity-gain application would require the full input range before the output saturates. However if the input signal has a large DC common-mode voltage, then a rail-to-rail input may be the only choice.

## Change in $V_{OS}$ with Input CMR



LMV710



LMC6482

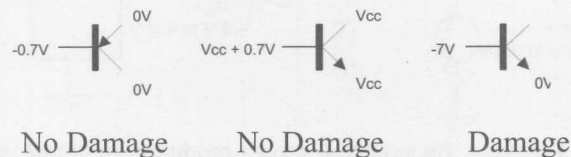


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Complementary input stages are available for CMOS Op-Amps, but these still show the same shift in offset voltage. When the application absolutely requires the input signal to swing through the transition region, you might want to consider the LMC6482. In this CMOS rail-to-rail Op-Amp the input stage uses wide compliance current mirrors and the body effect (MOSFETs are 4 terminal devices) to extend the performance of the P-channel inputs from below ground to 300 mV above the positive supply rail. An extra implant gives the PMOS pair a positive threshold voltage when the gates are near the positive supply (depletion mode FETs). The strong body effect moves the threshold from positive to negative as the gate voltage approaches the negative rail. A change in offset through the common-mode range still happens, but it is much smoother than the offset change for complementary input stages shown on the left.

## Input Stage Over Voltage



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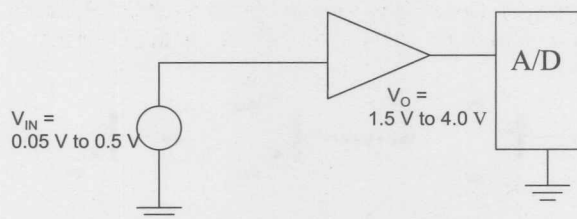
Whenever the input voltage is allowed to meet or exceed the supply rails the question arises as to how the Op-Amp will perform, and whether it can be damaged? Usually 200 mV to 300 mV above the rail will not cause abnormal operation and the datasheet will specify Abs Max ratings above which damage *may* occur. If the Op-Amp is un-powered but the signal source is powered then the application must be investigated more closely.

Typically as the supply limits are exceeded, a diode will be turned on, either by forward bias of a normally reverse biased diode or by reverse breakdown of a normally forward biased diode. For a PNP input when the input reaches 0.7 V below ground, the collector diode is turned on and current will flow. If this current is limited to a few mA ( $<10$  mA), then it is unlikely that damage will occur. However normal operation is not guaranteed since the current flow will be injecting stray electrons into the substrate of the device and transistors may turn on unpredictably. Similarly for an NPN input when the base voltage goes above collector voltage, it forward biases the collector diode and current will flow. Other circuits, such as ESD protection diodes, may affect how far the over-voltage can go.

While in the two previous instances damage can be avoided by limiting the current flow with resistors in series with the input leads, there is one case that will result in irreversible damage to the transistor. That is when the diode junction is taken into reverse breakdown. This is about 7 V for a typical NPN and, depending on the current level, the transistor will start to degrade until the diode ends up resembling a resistor. Even short, low-current breakdowns are serious since the effect is accumulative. The problem is less serious in low-voltage amplifiers, since the maximum supply voltage of 5 V is not large enough to reverse bias the diode (unless a high-speed process is used to fabricate the Op-Amp, when the reverse breakdown voltage may be as low as 3 V). It is even less likely with PNP transistors, which typically have a reverse breakdown voltage in excess of 30 V.



## Single-supply Op-Amp Biasing



**Problem:** An industrial sensor produces an output voltage proportional to temperature, pressure, flow, etc

$$V_{\text{low limit}} = 0.05 \text{ V}$$

$$V_{\text{high limit}} = 0.5 \text{ V}$$

Interface this to an A/D converter with an input range of 1.5 to 4.0 V



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Unlike conventional Op-Amps operating on split supplies where the input DC bias and output DC bias can both be at ground (0 V), biasing single supply Op-Amps is more of a challenge. Next we will look at several situations where an input-voltage range is converted to specified output-voltage range, usually for an ADC.

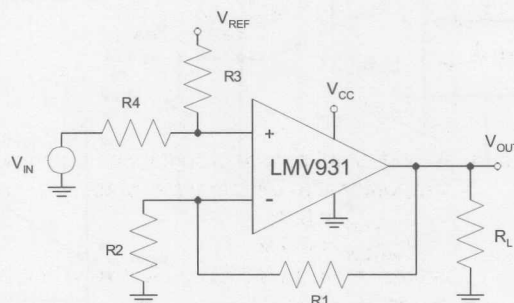
## What Is The Gain Of This Circuit?

Conditions:  $V_{CC} = 5V$

Choose a non-inverting, single supply, **DC-coupled** solution.

A single-supply Op-Amp will include the bottom rail (PNP input)

Both the  $V_{IN}$  and the  $V_{REF}$  voltage are inserted at the (+) input



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Sensor interface circuits of this type will be DC coupled. In this analysis, a separate voltage,  $V_{REF}$  will be used during the development of the formulas for generality. In the final circuit implementation, the  $V_{REF}$  point will normally be tied to the (+) plus rail, or  $V_{CC}$ . A rail-to-rail input circuit or a single supply Op-Amp with a PNP input should be chosen. The LMV931 is a rail-to-rail in, rail-to-rail out 1.8 to 5V Op-Amp.

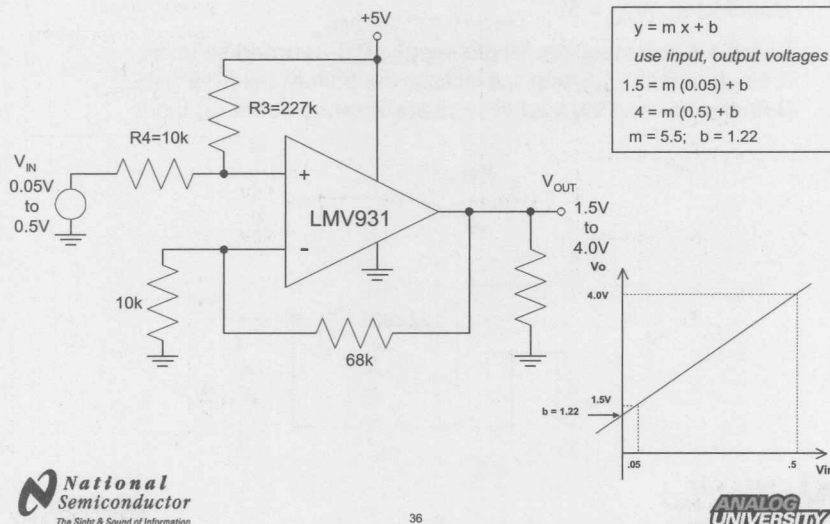
Shown here is an arrangement of external resistors that will accomplish the interfacing task.

We will use superposition to calculate the output of each of the following circuits. This assumption is correct because the terminals of an Op-Amp act as a summing junctions.

The gain of the circuit is determined by the ration of the feedback and source resistors at the inverting input as normal. That is,  $V_O = V_{IN} \times (1 + R1 / R2)$  for an input at the non-inverting terminal. For an input at the inverting terminal, the gain is  $- R1 / R2$ .

The design offset of the circuit is controlled by the ratio of resistors on the non-inverting input.

## Final Circuit with Component Values



The graph in the lower right corner and the calculations in the box in the upper right produce values for the gain ( $m$ ), and the offset ( $y$ -intercept). Since the application provides two input and output points, we use simultaneous equations to calculate the two needed parameters. In this case, both of the calculated quantities,  $m$  and  $b$ , have a positive sign. Therefore, both the input signal,  $V_{IN}$  and the offset signal, generated by the resistor divider  $R3$  and  $R4$ , are inserted at the non-inverting input. By superposition, the two add to form the output signal.

What is the gain of this circuit?

Superposition; write  $V_O$ ,  $V_{REF}$  equation separately.

1.  $V_O = V_{IN}(R3/(R3+R4))(1+R1/R2)$ , and for  $V_{ref}$
2.  $V_O = V_{REF}(R4/(R3+R4))(1+R1/R2)$  and rewrite,  $(1+R1/R2)$  as  $(R1+R2)/R2$   
then by superposition,
3.  $V_O = V_{IN}(R3/(R3+R4))((R1+R2)/R2) + V_{ref}(R4/(R3+R4))((R1+R2)/R2)$

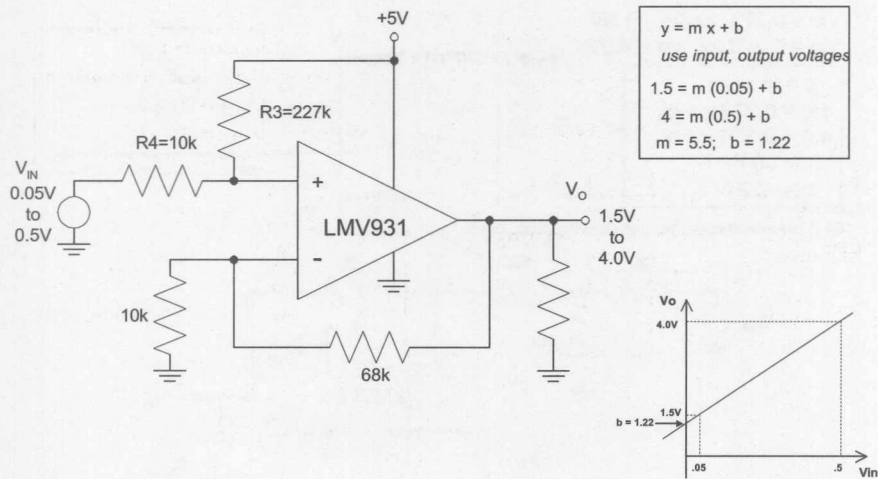
NOW: the first term is a proportionality term dependent on the input (gain)

because  $V_{REF}$  will turn out to be fixed (+5V). The second term is a constant.

This makes the  $V$  equation of the form:

4.  $y = mx + b$  (this looks familiar) so by inspection, rewrite from 1), 2)
  5.  $m = (R3/(R3+R4))((R1+R2)/R2)$
  6.  $b = V_{REF}(R4/(R1+R2))((R1+R2)/R2)$  and calculate; for our two points, (eq. 4)
  7.  $V_O = 1.5, 4.0V$  for  $V_{IN} = 0.05, 0.5V$
  8.  $1.5 = m(0.05) + b$
  9.  $4 = m(0.5) + b$
- and  $m = 5.55, b = 1.22$

## Final Circuit with Component Values



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(continued from prior slide) then

$$10) V_O = 5.55V_{in} + 1.22$$

Now, choose resistor values and solve eq. 5 and 6 separately for  $(R_1 + R_2)/R_2$

$$11) m = R_3 / (R_3 + R_4) \cdot (D)$$

$$12) b = V_{REF} \cdot R_4 / (R_3 + R_4) \cdot (D)$$

$$m / (R_3 / (R_3 + R_4)) = b / V_{REF} \cdot (R_4 / (R_3 + R_4)). \text{ Then,}$$

$$13) m \cdot V_{REF} \cdot R_4 = b \cdot R_3$$

$$14) R_3 = (m/b) V_{REF} \cdot R_4. \text{ For our example,}$$

$$R_3 = (5.55/1.22)(5)(R_4)$$

$$15) R_3 = 22.7R_4$$

Let  $R_4 = 10K$ , then  $R_3 = 227K$  and the ratio of  $R_1$  to  $R_2$ , is calculated from 10 (or 9).

$$\text{Remember } D = (R_1 + R_2)/R_2$$

$$15) (R_1 + R_2)/R_2 = m(R_4 + R_3)/R_3$$

$$\text{then, } (R_1 + R_2)/R_2 = 5.55(227K + 10K)/227K$$

$$(R_1 + R_2)/R_2 = 5.80 \text{ and}$$

$$16. R_1 = 6.80R_2$$

again, choose  $R_2 = 10K$ , then  $R_1 = 68K$

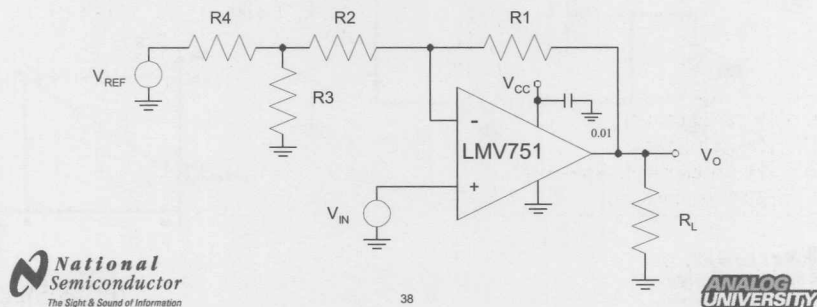
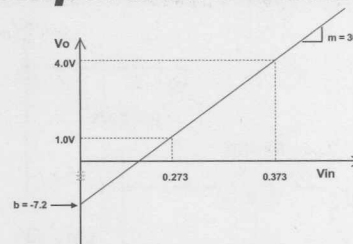
## Example 2: Kelvin Temperature Sensor

$V_{IN} = 0.273$ , for  $V_O = 1.0V$

$V_{IN} = 0.373$  for  $V_O = 4.0V$

$$\begin{aligned} y &= mx + b \\ 1.0 &= 0.273x + b \\ 4.0 &= 0.373x + b \\ m &= 30 \\ b &= -7.2 \end{aligned}$$

for  $b$  (intercept) negative, use modified bias circuit.



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Now, let's do a second case. This is a Kelvin temperature sensor example. Consequently there is a large offset in the physical situation. Again, this sensor will be interfaced to an ADC.

The LMV751 is a single-supply low-noise, CMOS input Op-Amp, with an input range that includes the ground rail. The output is rail-to-rail.

Notice at the outset that the input voltage is at the non-inverting terminal, and the offset term is at the inverting input. The reason for this will be seen in the development. What is the meaning of the  $-b$  (intercept) term? The figure in the upper right illustrates the condition. We need not be concerned about the negative  $V_O$  voltage because it is outside the range of interest, and the Op-Amp does not have to produce the negative voltage.

In this case,  $y = mx - b$  and the negative sign for  $b$  means we insert  $V_{REF}$  at the inverting input. Since the gain is inverting, this gives it a negative sign.

Again use superposition,

$$V_O = V_{IN} * m - b$$

On the plus input, the contribution to  $V_O$  is,

$$17) V_{IN} * (1 + R1 / (R2 + R4 \parallel R3)) \quad 16), \text{ or}$$

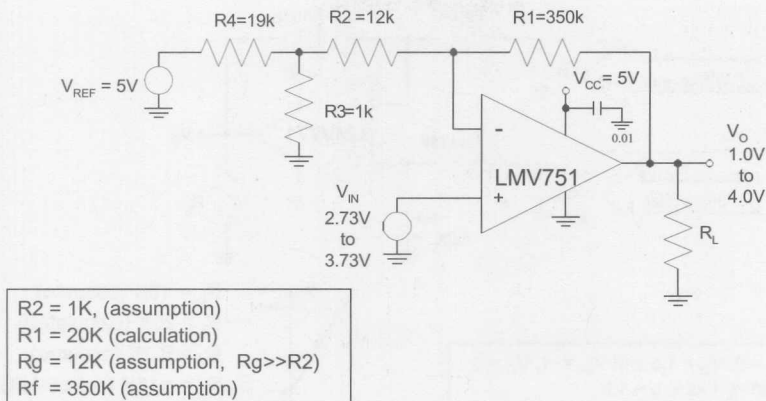
$$18) V_{IN} * (R1 + R2 + R1 \parallel R2) / (R2 + R4 \parallel R3) \text{ on the minus input, the contribution to output is}$$

$$19) - V_{REF} * (R3 / (R3 + R4)) * (R1 / (R2 + R4 \parallel R3)), \text{ by inspection,}$$

$$20) m = (R1 + R2 + R4 / R3) / (R1 + R4 \parallel R3)$$

$$21) \text{abs}[b] = V_{REF} \{ R3 / (R3 + R4) \} * \{ R1 / (R2 + R4 \parallel R3) \}$$

## Final Circuit for Example 2: Temperature Sensor to A/D Converter



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(example 2 continued)

22)  $V_O = 30V_{IN} - 7.2$

$m = (R_1 + R_2 + R_4/R_3)/(R_2 + R_4/R_3)$ , by examining  $m$ , make some simplifying assumptions

a)  $R_4 \gg R_3$ , because  $V_{IN}$  is near the bottom rail

b)  $R_1 \gg R_2$ , because we know gain is high (30)

c) if we make  $R_4 < R_2$ , then  $R_4/R_3$  will be negligible in the equation for  $m$

notice that our  $R$  values will span 3 orders of magnitude. Start by choosing,  $R_3 = 1K$  and  $R_2 = 12K$ , from c), then the  $m$  equation becomes,

23)  $m = (R_1 + R_2)/2$  because  $R_2 \gg R_4$ .  $(R_1 + R_2)/R_2 = 30$ .

24)  $R_1 = 29R_2$  then,  $R_2 = 12K$ ,  $R_1 = 350K$ . Next, calculate  $R_4$ , using b

$abs[b] = V_{REF} * \{R_3/(R_4 + R_3)\} * \{(R_1/(R_2 + R_4/R_3))\}$  this reduces to,

25)  $abs[b] = V_{REF} * \{R_3/(R_4 + R_3)\} * (R_1/R_2)$  for our assumptions  $R_2 \ll R_g$

then,  $abs[7.2] = 5 \{R_3/(R_4 + R_3)\} (350K/12K)$

$R_4 = 19R_3$

$R_4 = 19K$

Summarizing;

$R_3 = 1K$ , (assumption)

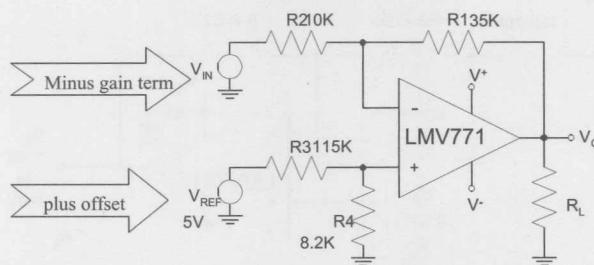
$R_4 = 19K$  (calculation)

$R_2 = 12K$  (assumption,  $R_2 \gg R_3$ )

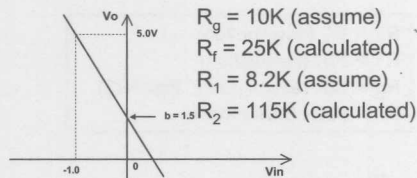
$R_1 = 350K$  (calculation)

### Example 3.

$$V_o = -m V_{in} + b \text{ (- gain, + intercept)}$$



$V_{IN} = 0, V_O = 1.5$  and  $V_{IN} = -1, V_O = 5$   
then  $m = -3.5, b = 1.5$



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Here the LMV771 is shown. This is a low-voltage, rail-to-rail out Op-Amp whose input range includes the negative rail.

Proceeding with superposition as in the other examples,

$$V_O = -V_{IN}(R_1/R_2) + V_{REF}(R_4/(R_4+R_3))\{R_1+R_2\}/R_2$$

by inspection,  $\text{abs}[m] = R_1/R_2$

$$b = V_{REF}(R_4/(R_4+R_3))\{R_1+R_2\}/R_2$$

CASE 3 Example:

$V_{IN} = 0, V_O = 1.5$  and  $V_{IN} = -1, V_O = 5$ , then  $m = -3.5, b = 1.5$

$V_O = -3.5V_{IN} + 1.5$  then from prior equations,

$$\text{abs}\{-3.5\} = R_1/R_2$$

$R_1 = R_2(3.5)$ ; choose  $R_2 = 10K$ , then  $R_1 = 35K$ , from Eq. 'for  $b$ ,

$b = V_{REF}((35K+10K)/10K)(R_4/(R_4+R_3))$ , let  $V_{REF} = 5v$ , then  $R_3 = 14R_4$ .  $R_2 = 10K$  (assume),  $R_1 = 35K$  (calculated),  $R_4 = 8.2K$  (assume),  $R_3 = 115K$  (calculated).

What is the meaning of the minus input term? Can a single-supply circuit accommodate a minus input?

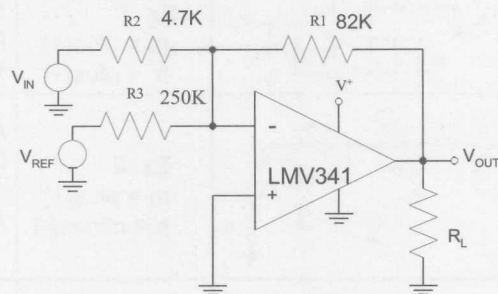
The answer is yes. The circuit will operate correctly provided that the input source itself can supply a minus voltage. As to the Op-Amp circuit, the minus input is on the inverting input, which is biased by the calculated resistors, above ground. Since this is a summing junction and the input voltage generator is isolated from the minus input by the 10K resistor, the circuit will work as described.

$R_2 = 10K$   
 $R_1 = 35K$   
 $R_4 = 8.2K$   
 $R_3 = 115K$

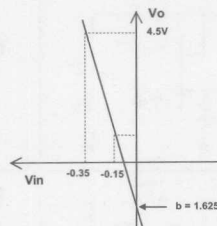


## Example 4.

**$V_o = -m V_{in} - b$  (- gain, - intercept)**



Ex.  $V_{in} = -0.15 \text{ V}$ ,  $V_o = 1.0 \text{ V}$   
 $V_{in} = -0.35 \text{ V}$ ,  $V_o = 4.5 \text{ V}$   
 $1 = -.15m + b$   
 $4.5 = -.35m + b$ ,  
 then  $m = -17.5$ , and  $b = -1.625$



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The LMV341 is a rail-to-rail out, low voltage, Op-Amp. The input includes the minus rail.

$V_o = -V_{in}(R_1/R_2) - V_{REF}(R_1/R_3)$  (superposition)

$\text{abs}\{m\} = R_1/R_2$

$\text{abs}\{b\} = V_{REF}(R_1/R_3)$

Ex.  $V_{in} = -0.15 \text{ V}$ ,  $V_o = 1.0 \text{ V}$

$V_{in} = -0.35 \text{ V}$ ,  $V_o = 4.5 \text{ V}$

$1 = -0.15m + b$

$4.5 = -0.35m + b$ , then  $m = -17.5$ , and  $b = -1.625$

then  $\text{abs}\{m\} = 17.5 = R_1/R_2$

Now, by inspection, we would like the signal chain resistors to be small compared to the offset resistors. Choose  $R_2 = 4.7 \text{ K}$ , then  $R_1 = 17.5(4.7 \text{ K}) = 82 \text{ K}$

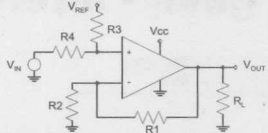
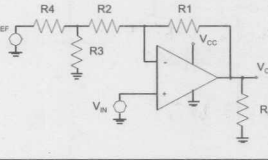
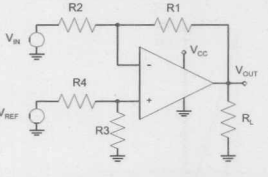
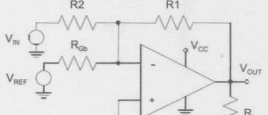
Now, calculate  $R_3$  from  $b$ ,  $\text{abs}\{b\} = V_{REF}(R_1/R_3)$ , let  $V_{REF} = 5 \text{ V}$

$b = 1.625 = 5(82 \text{ K})/R_3$

$R_3 = 250 \text{ K}$ ,  $R_2 = 4.7 \text{ K}$  (assumed),  $R_1 = 82 \text{ K}$  (calculated)



## SUMMARY – Single-Supply Biasing

<b>Ex 1</b> $V_o = +V_{in} + V_{dc}$		$y = mx + b$ <b>Ex. 1</b> $m = \text{plus}(+)$ $b = \text{plus}(+)$	$R2 = (m/b)V_{REF} * R4$ $R1 = R2 * (m-1)/D$ Where $D = R3/(R3+R4)$
<b>Ex. 2</b> $V_o = +V_{in} - V_{dc}$		<b>Ex. 2</b> $m = \text{plus}(+)$ $b = \text{minus}(-)$	<b>Assumptions:</b> $R4 > R3, R1 > R2, R4 < R2$ $m = (R1+R2)/R2$ $Abs\{b\} = (V_{REF}/D) * R1/R2$ $D = R3/(R4+R3)$
<b>Ex 3</b> $V_o = -V_{in} + V_{dc}$		<b>Ex. 3</b> $m = \text{minus}(-)$ $b = \text{plus}(+)$	$abs\{m\} = R1/R2$ $R3 = R4[(V_{REF}/bE)-1]$ $E = R2/(R1+R2)$
<b>Ex. 4</b> $V_o = -V_{in} - V_{dc}$		<b>Ex. 4</b> $m = \text{minus}(-)$ $b = \text{minus}(-)$	$abs\{m\} = R1/R2$ $abs\{b\} = V_{REF}(R1/R3)$

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## **Stability Issues**

- **Oscillators Don't!**
- **Amplifiers Do!**



1



As Bob Pease is fond of saying “Oscillators don’t, Amplifiers do.....oscillate that is.”

When an Op-Amp is first hooked up, it may or may not work quite as expected. If the supply current is much higher than expected, or the package feels warmer than the anticipated power dissipation calculations would indicate, then the amplifier is probably oscillating. When a fast pulse signal is applied and the output waveform shows excessive overshoot and ringing, then the device may be close to oscillating.

## ***Oscillation Causes***

- **Is the frequency close to  $f_u$ ?**
- **Are long supply leads being used?**
- **Are the bypass capacitors close to the pin?**
- **Has the ground plane been removed under the input pins?**
- **Does the output lead pass close to the inverting input?**
- **Do the inputs and outputs share a common ground lead?**



2



The first step in trouble shooting stability problems is to look at the frequency of oscillation. If the frequency is not close to  $f_u$ , the unity-gain crossover frequency of the Op-Amp, then the feedback loop is not the culprit. Instead, the source of the oscillation lies elsewhere.

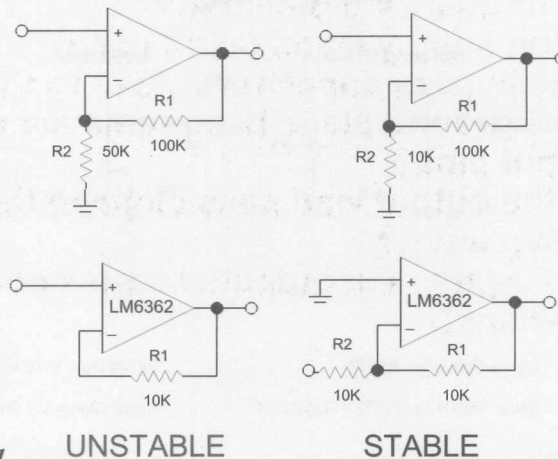
Long power supply leads are inductive. A 22-gauge wire looks resistive at low frequencies, 0.02  $\Omega/\text{ft}$ , but the parasitic inductance of 20 nH/ft will cause it to look inductive above 160 kHz. This inductance in conjunction with the typical ceramic bypass capacitor will create resonant circuits in the megahertz range.

Printed circuit board traces from the output components running close to the inverting input should be avoided, and even when ground planes are used, the ground plane should be cleared away from the vicinity of the inverting input.

Ground loops can cause high distortion, if not oscillations, so output component ground wires that carry high currents should return to the system ground separately from the input component ground wires.

Even when the circuit is not actually oscillating, higher than expected distortion levels are an indication that something is not right.

## Feedback Network Instability



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If you suspect the instability is caused by the feedback network, then temporarily increase the closed-loop gain (by a factor of two to four for example). If the increase in closed-loop gain does not stop or at least decrease the frequency of oscillation, then the problem is elsewhere.

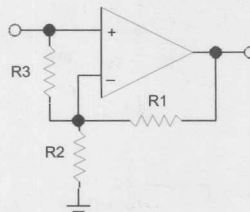
A fairly common problem with feedback loop instability occurs with the voltage follower where, in the case of the non-inverting follower, there is 100% feedback of the output signal to the inverting input. Some amplifiers will be unstable in this configuration, yet stable in the inverting follower configuration. This is because of the difference in closed-loop bandwidth between the inverting and non-inverting configurations discussed earlier.

Of course, other amplifiers in the follower configuration will be unstable both inverting and non-inverting. Audio Op-Amps will fall into this category and are often specified to be stable with closed-loop gains of 20 dB (X10) or more. High-speed uncompensated amplifiers intended to be used at high gain settings are not always unity-gain stable.

If the sacrifice in closed-loop bandwidth and input sensitivity is acceptable, then a signal pad or attenuator will allow the same overall system gain with the amplifier operating at a higher gain.

## Improving Amplifier Stability

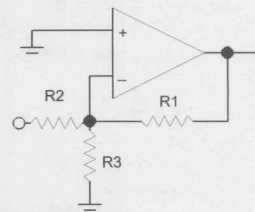
NON-INVERTING



$$\text{Signal Gain} = 1 + R1/R2$$

$$\text{Noise Gain} = 1 + R1(R2 + R3)/R2R3$$

INVERTING



$$\text{Signal Gain} = -R1/R2$$

$$\text{Noise Gain} = 1 + R1(R2 + R3)/R2R3$$

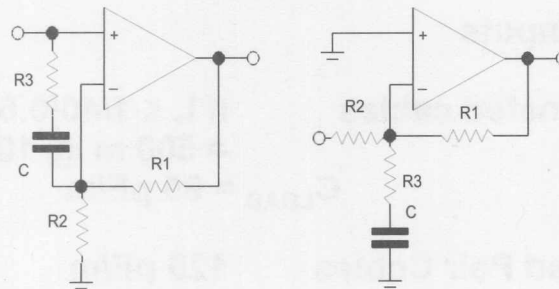
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If a resistor is connected between the Op Amp inputs that is much smaller (1/10) than the feedback resistor R1, then the noise gain can be reduced to a value that ensures stability without changing the signal gain.

## Avoiding Offset Errors



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A drawback to raising the noise gain is that the DC offset ( $V_{os}$ ) and input noise of the amplifier are also raised by the value of the noise gain. Putting C in series with R3 eliminates the offset voltage increase and puts the AC noise components up into a region above the corner frequency set by  $1/2\pi R3C$ . As with most "fixes," the actual values are empirically derived and will depend on a particular application and Op-Amp type.

## Capacitive Loads

- ADC inputs
- Terminated cables      if  $L \leq 1/40(0.66 \text{ c/f})$   
                                      = 500 m @ 10 kHz  
                                       $C_{\text{LOAD}} = 95 \text{ pF/m}$
- Twisted Pair Cables      120 pF/m



6



The majority of Op-Amps, even high-speed, are designed to be *unity-gain stable*, that is, with 100% feedback they will not oscillate. If that is the case, why should the amplifier ever oscillate with purely resistive components in the feedback path? We have already looked at the case of capacitance at the inverting input being able to introduce phase shifts that will cause loop instability at high frequencies within the Op-Amp open-loop bandwidth. A more common cause of feedback instability is a capacitive load.

Sometimes the capacitance is readily identified by inspection of the circuit schematic - is the Op-Amp driving the input of an ADC for example? Often the capacitive load is less easy to identify, and this is why oscillations become an unanticipated problem.

Terminated co-axial cables are usually thought to be resistive, but if the cable length  $L$  is less than  $1/40$  of the signal wavelength being transmitted, then it will look capacitive at that frequency.

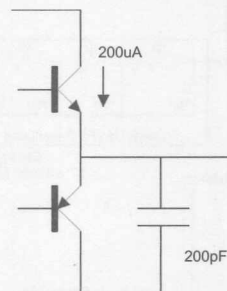
22 gauge twisted pair cables bundled together can have a capacitive loading effect of 40 pF/ft.

Realizing that most general purpose Op Amps are guaranteed stable with 200 pF loads, it is easy to see why designers can get into trouble.

Note:

Sometimes the reverse is true, What appears to be a capacitive load turns out not to be so bad after all. See the TFT Vcom driver application shown later.

## Capacitive Loads



$$R_o = r_e / 2 = 65 \, \Omega$$

$$f_c = 1 / 2\pi R_o C_o = 12 \, \text{MHz}$$

$$\text{Lag} = \tan^{-1}(10 \, \text{MHz} / 12 \, \text{MHz}) \\ = 40 \, \text{degrees}$$

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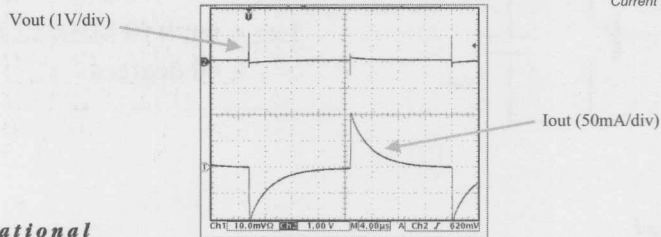
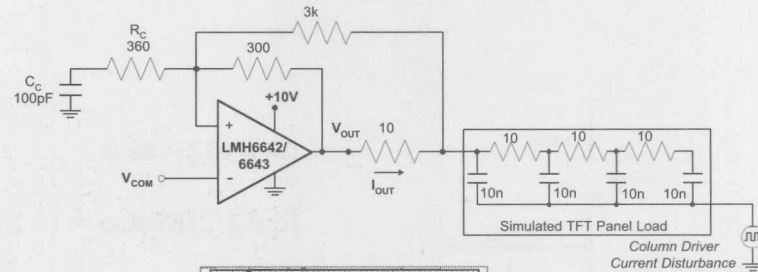
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The reason capacitive loads are an issue is the open-loop output resistance of the Op-Amp. At frequencies where the loop is closed, the output resistance is divided by the loop gain and is a very small value indeed. Open-loop the output resistance is the dynamic emitter resistance ( $r_e$ ) of the output transistors, and the size of this depends on the bias current flowing in those transistors. Together with the load capacitance, the output resistance forms a low pass RC filter with a phase lag at a frequency  $f$  given by  $\phi = \tan^{-1}(f/f_c)$ .

If the output resistance is  $65\Omega$  and the load is  $200 \, \text{pF}$  then  $f_c = 1 / 2\pi \cdot 65 \cdot 200 \cdot 10^{-12} = 12 \, \text{MHz}$  which will introduce an additional phase lag of  $40 \, \text{degrees}$  at  $f_u$  if the unity-gain crossover frequency of the amplifier is  $10 \, \text{MHz}$ .



## Driving TFT Panel $V_{COM}$

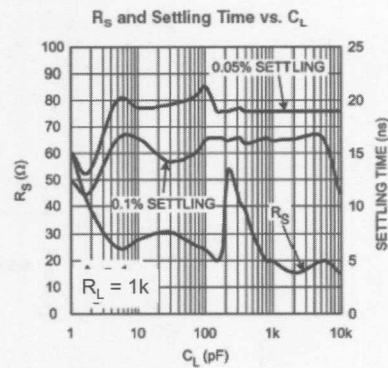
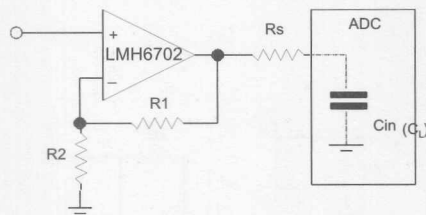


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In a TFT panel, the back plate of every pixel is connected to a common voltage known as Vcom, and Op-Amps are used to maintain this voltage as the pixels are turned on and off with the display requirements. Each column of pixels has between 16 pF to 33 pF stray capacitance and the total capacitance may add up to 25 nF to 100 nF. The Op-Amp must have a high current output and slew rate to charge this capacitance. Fortunately for stability in this case, the capacitance is distributed along the entire length of each column which has a 2 Kohm to 40 Kohm resistance. Therefore the load (including the rows) is a distributed RC network with a total capacitance of 50 nF to 200 nF. Although the capacitance will place an additional pole in the feedback loop, the resistance will create a zero to cancel the effect of this pole. This zero, at a frequency from 8 KHz to 160 KHz, is well below the Op-Amp unity-gain crossover frequency  $f_u$ , and the amplifier remains stable without additional compensation.

## CFB Op-Amp Stabilization



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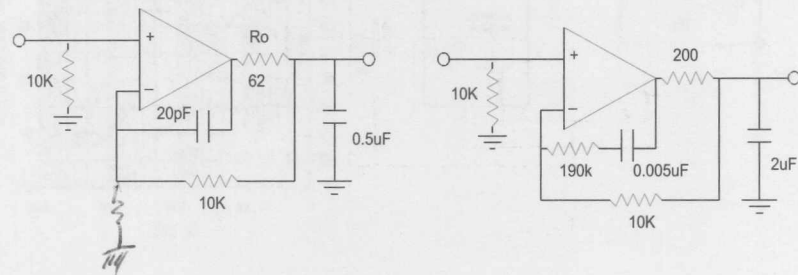
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In the more general case of a capacitance load of a few hundred picofarads, some form of external compensation may need to be added, if only to reduce overshoot and ringing. With a CFB Op-Amp, often the only solution is isolation of the load with a small damping resistor  $R_S$  in series with the output. Here the choice of specific values will depend on the load capacitance, the particular Op-Amp being used, and the type of response desired. If fast settling is required, the size of the resistor will go up, but this will affect the output swing and slew rate. If overshoot and slower settling is acceptable, then smaller resistors can be used with an improvement in signal bandwidth. Higher values of closed-loop gain will ease the choice of a suitable (small) resistor. Resistor values will range from about 10 Ohm to as much as 300 Ohm, depending on the load and the particular Op-Amp.

The example shown here assumes a relatively light load of 1 Kohm. In general, the fast slewing of a CFB Op-Amp with a heavy load will allow the size of  $R_S$  to be reduced for a given settling time.

## VFB Op-Amp Stabilization



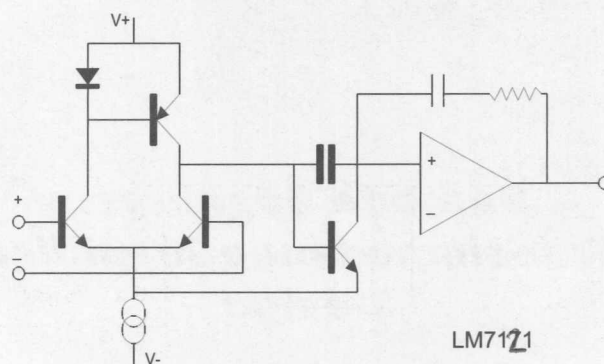
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For a VFB Op-Amp, the resistor can be placed inside the feedback loop and, as such, will have no impact on the output load swing or the slew rate at frequencies inside the closed loop bandwidth. At high frequencies, the 20 pF capacitor provides direct feedback and because of the 62 Ohm isolating resistor it does not have the phase lag associated with the load. Again, appropriate values are determined empirically and the components shown are given simply as a starting point.

## Automatic Compensation



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When the capacitive load is unknown or likely to change, Op-Amps such as the LM7121 can be used. This class of Op-Amps is stable driving unlimited capacitive loads. The concept is shown above.

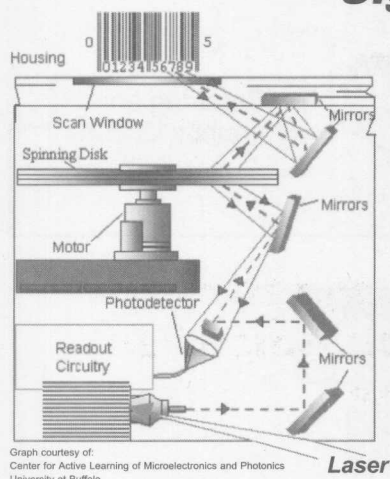
Stability compensation of the amplifier is provided by the Miller capacitance of the second gain stage. The output stage is simple a unity-gain buffer. Any signal at the input to the buffer is faithfully reproduced at the output. If a capacitor is placed from the buffer input to output, under normal operation both sides of the capacitor see the same voltage and it is as if the capacitor wasn't even in the circuit. At high frequencies with a capacitive load, the phase lag generated at the output by the load will cause a voltage to appear across the feedback capacitor effectively placing a small capacitance in parallel with the Miller capacitance. As more capacitance is placed in parallel, the amplifier GBW is reduced and the amplifier remains stable.

One thing to bear in mind, as the closed-loop bandwidth is reduced, this can cause higher distortion in the signal at high frequencies compared to a similar Op-Amp without this internal network. In general, if low distortion is important, then choosing a more conventional output stage with compensation tailored to the specific load is a better choice.



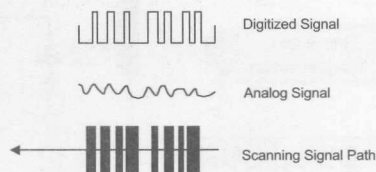
## **Barcode Scanners: Transimpedance Amplifier Design**

# Converting Symbols Into Electrical Signals



Graph courtesy of:  
Center for Active Learning of Microelectronics and Photonics  
University at Buffalo

Laser



ID data is encoded in the barcode symbol

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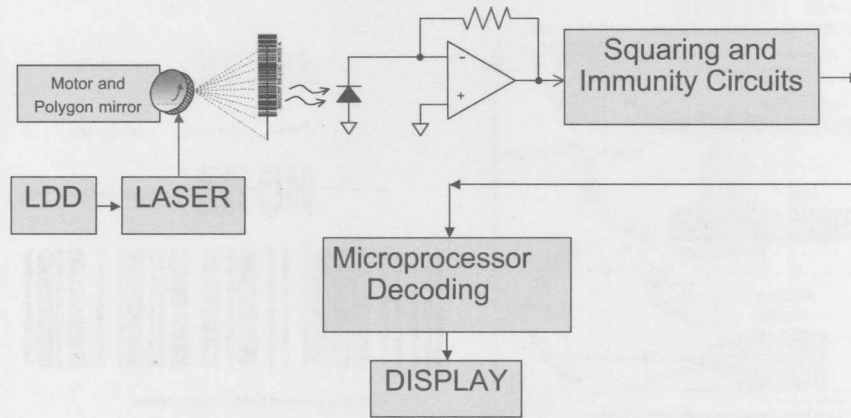
## Barcode Scanners

The function of the barcode scanner is to "read the information" represented in the image of the barcode. In its most basic form, the scanner/detector captures the absence or presence of light in the code's bars and spaces. The detector circuitry measures the width of lines contained in barcode symbols to an accuracy that minimizes uncertainties in making the decision as to whether a bar or space is present. The processed analog signal is then digitized and translated into recognizable or computer-compatible data. This data is transmitted to a computer for comparison with a database that contains useful pricing, inventory, and other information that is uniquely associated with the item being scanned.

Schematically shown above are the simplified elements of a barcode scanner system. The dashed blue lines in the pictorial on the left trace the laser scanning signal. This outgoing signal traverses a system of mirrors and finally scans the barcode of the item in the reading window of the scanner. The repetition rate of the scanning signal is controlled by the stepper-motor driven rotating disc. The z dimension of the disc is machined to a regular polygon shape such that the laser signal is spatial spread by the flattened sides of the spinning disc. This mechanical action creates the scanning signal. The number of scans-per-second is controlled by the speed of rotation of the disc. The solid red lines indicate the returning signal encoded with the information in the barcode symbol. This optical signal returns through a system of mirrors and impinges on the photodetector as shown. The amplifier used to aid in recovery of the signal out of the photodetector, the transimpedance amplifier, is the object of this analysis. Essentially, this circuitry is part of the signal processing that converts the analog signal shown at the right into the digitized signal shown at top right. A typical barcode symbol is shown on the right.

Two-dimensional barcodes are also becoming popular and carry a far greater amount of information. These barcodes require a raster scanning system or, alternately, are read using an imager, such as a CCD device.

## Barcode Scanner Block Diagram



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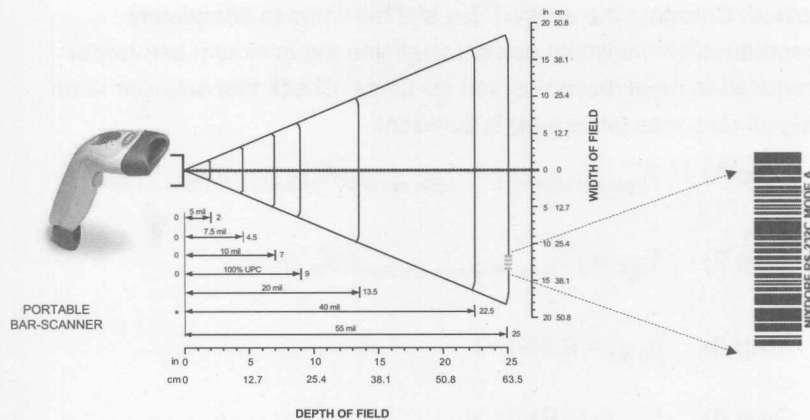
14

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This analysis will focus on the detector side of the barcode equipment represented by the Op-Amp, as shown. The scanner side circuitry consists essentially of a laser diode driver and the laser itself. The detector side circuitry consists first of an amplifier that accepts the diode detector current generated by the laser beam signal that has been reflected from the barcode symbol. This is the transimpedance amplifier (TIA) and will be the object of this analysis. The detected signal is amplified in the TIA and emerges at an appropriate level for the squaring and immunity circuits. These analog circuits are a combination of filters and comparators. They create a square wave signal that is immune from false triggering and spurious signals generated in the scanning and detecting process. Many different approaches are employed to ensure a reliable and readable square-wave signal for analysis by the microprocessor, for ultimate display by the scanner.



## Portable Bar Scanner Optical Range



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Portable barcode scanners have become the workhouse instrument in terms of identifying barcode-symbol tagged items. The barcode scanner has a scanning range that is defined by the manufacturer. A typical spacial aspect for operation of a handheld portable is 15 in (63.5 cm) in the dimension of depth of field, and 20 in (50.8 cm) in the dimension of width of field. An estimate of the speed of response for a barcode symbol at the outer limit of both depth and width will be made and from this the necessary amplifier bandwidth will be calculated. A standard barcode standard will be used for this example and the scans-per-second will be from a manufacturer's specifications for a unit. Shown on the right is a generic barcode symbol.



## **Finding Transimpedance Bandwidth for Barcode**

Method: Calculate the desired rise and fall times to adequately reproduce the minimum pulse. Determine the minimum bandwidth required to meet these rise and fall times. Check that amplifier large signal response (slew rate) is sufficient.

$$\text{Step 1) } T_{\text{scan min element}} = t_{\text{scan symbol}}(K_{\text{field depth}})(K_{\text{min element}})$$

$$\text{Step 2) } T_{R,F} = (T_{\text{scan minimum element}})(K_{R,F})$$

$$\text{Step 3) } f_{-3\text{ dB}} = 0.35/t_r$$

$$\text{Step 4) } f_{\text{max}} = (\text{SR})/2\pi V_P$$



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The mechanical aspects of the scanning operation will be used to determine the bandwidth, from now on called the transimpedance bandwidth, for the barcode scanner. The amplifier will be a transimpedance amplifier because the input is a current – from the photodetector – and the output is a voltage. The method to be used is outlined above. If the rate of change of the fastest optical signal from the detector can be estimated, a computation of the response time needed by the operational amplifier in the TIA mode can be made. Calculation of final values in the TIA application will then complete the design example.

Included in the estimation is the field depth, the scan repetition rate, the symbol dimensions and the width of the minimum element in the scan. The factor  $K_{R,F}$  accounts for the desired time for the output pulse to reach the maximum amplitude and then fall back to zero.

## Finding Transimpedance Bandwidth for Barcode - Definitions

Code 39 Barcode parameters  
1 standard symbol width = 3.6 cm (36 mm)  
Minimum element width = 0.191 mm (.0077 in)

Portable Scanner Dimensions (see Figure)  
scans/sec. = 44  
Max field depth = 63.5 cm.(25 in.)  
Max field width = 80 cm  
Field depth at Code 39 symbol  
width of 3.6 cm = 5.5 cm depth

Scan symbol width



Minimum element width



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Many barcode standards are commonly used today, and the legacy of each of these remains. Common codes are Code 39, Codabar, ITF UPC/EAN, and Code 128. For this example, we will use an early industrial standard called Code 39. Each character in Code 39 is made up of 9 bars – 3 of which are wider than the others, hence Code 39. A single character consists of 5 black bars and 4 white bars. The space between each barcode character is called the inter-character gap. Its width is undefined, but is usually equivalent to a narrow white bar. The task here in determining the application bandwidth will focus on the amplifiers response to the minimum element width, such as a narrow white bar.

The portable scanner repetition rate to be used will be 44 scans/second. Scan rates vary widely for barcode equipment from basic rates, such as in this example, up to thousands of scans/second in the highest performance models.

## ***Finding Transimpedance Bandwidth – Minimum Symbol Scan-time***

### **Step 1. Calculate time to scan minimum symbol element**

$$T_{\text{scan minimum element}} = (t_{\text{scan symbol}})(K_{\text{field depth}})(K_{\text{min element}})$$

Refer to plan figure;  $T_{\text{scan symbol}} = 1/\text{scans per second}$

$$\begin{aligned} K_{\text{field depth}} &= \text{symbol width}/\text{max field width} \\ &= 3.6 \text{ cm}/80 \text{ cm} \\ &= 0.045 \end{aligned}$$

$$\begin{aligned} K_{\text{min element}} &= \text{min element width}/\text{symbol width} \\ &= 0.191 \text{ mm}/36 \text{ mm} \text{ (Code 39 standard)} \\ &= 0.00531 \end{aligned}$$

$$T_{\text{scan minimum element}} = (1/44)(3.6 \text{ cm}/80 \text{ cm})(0.191 \text{ mm}/36 \text{ mm})$$

$$T_{\text{scan minimum element}} = 5.4 \text{ } \mu\text{s}$$



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How much time does it take for the barcode scanner to scan the minimum element of a barcode symbol at the maximum field depth? This is the first calculation needed in our analysis.

1) Defines the time to scan a minimum element. For our example, the field depth factor, Kfd is represented by the width of the Code 39 symbol, divided by the overall width of the scanning field.

2)  $K_{fd} = 3.6 \text{ cm}/80 \text{ cm} = 0.045$ .

3) We determine the a factor defining the width of a minimum barcode symbol element, compared to the overall width of the symbol. For Code 39, this is  $0.191 \text{ mm}/36 \text{ mm} = 0.00531$

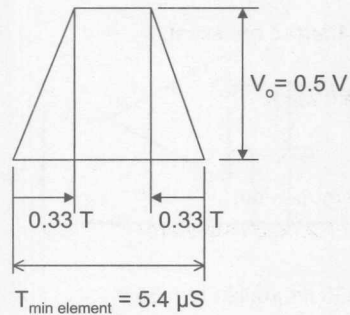
4) Now, the scan time for the minimum width symbol element in a Code 39 standard symbol at maximum field depth is given. This equation modifies the scan time for the particular portable barcode, which in our example is 44 scans per second, 1/44 or 0.023 seconds.

5) Applying the factors identified and calculated above, yields the minimum element scan time at maximum scan depth as 5.4 microseconds.

A factor not considered here, but which could be, is the "yaw" at the time of scan. The tilt angle (pitch) does not affect the overall minimum element scan time, but the yaw angle does. Acceptable angles are in the range of 30 degrees. Inclusion of this factor would result in a lower scan minimum scan time and therefore, a higher application bandwidth.

## ***Finding Transimpedance Bandwidth – Rise and Fall Time***

**STEP 2. Determine rise and fall time.**



Assume  $t_{\text{rise}}$  and  $t_{\text{fall}} = 33\%$  of total scan time for minimum element width in symbol

$$T_{R,F} = (T_{\text{scan minimum element}})(K_{R,F})$$

$$K_{R,F} = 0.33$$

$$T_{R,F} = (5.4 \mu\text{sec})(0.33)$$

$$T_{R,F} = 1.8 \mu\text{S}$$



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Now in the interest of not over-designing the application circuitry, an assumption is made concerning what rise and fall times are needed to successfully scan the minimum element. In this example, we have assumed a rise and fall time of 1/3 each of the total minimum element scan time.

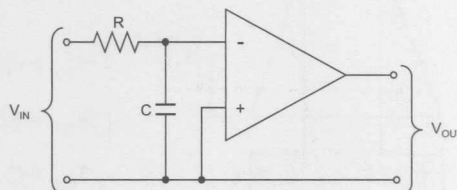
From this the rise and fall times for the example are calculated, that is  $0.33 \times 5.4 \mu\text{sec} = 1.8 \mu\text{sec}$ .

## Finding Transimpedance Bandwidth- Signal Bandwidth

### Step 3. Calculate the bandwidth

For single pole roll-off;

$$\begin{aligned} f_{-3\text{ dB}} &= 0.35/t_r \\ &= 0.35/1.8 \times 10^{-6} \\ &= 194.4 \text{ kHz} \end{aligned}$$



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An Op-Amp can be modeled as an amplifier with an infinite bandwidth preceded by a single pole RC filter network as seen in the above figure. This filter is due to the compensation in the mid-stage of an Op-Amp discussed earlier.

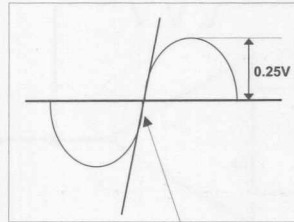
For a single pole filter of this type, we calculate the rise and fall time from the network time constant RC. 10% of the maximum occurs in 0.1RC and 90 in 2.3RC. Therefore the rise (or fall) time is 2.2RC and

$$t_r = t_f = 0.35/f_{-3\text{ dB}}$$

With a rise time of 1.8  $\mu$ Sec, the minimum bandwidth is 194.4 kHz.

## Large Signal Response

### Step 4. Check the slew rate



Let max slope = slew-rate

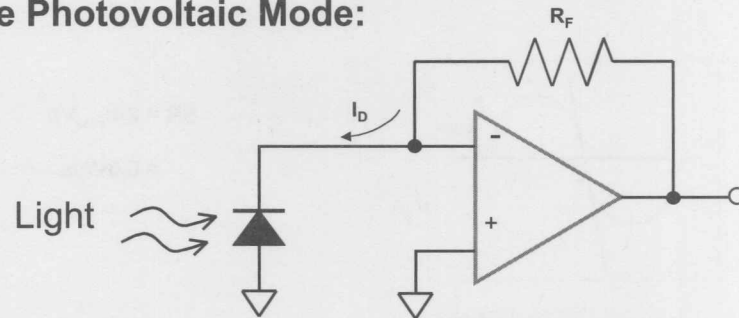
$$\begin{aligned} SR &= 2\pi f_{\max} V_p \\ &= 0.3\text{V}/\mu\text{s} \end{aligned}$$

The signal bandwidth we have just derived is the minimum bandwidth for the system. The Op-Amp bandwidth will need to be greater than this and other factors, such as stabilization and large signal performance will enter into the calculations. We will discuss stabilizing transimpedance amplifiers later on, but the large signal performance of an Op-Amp is determined in part by its slew rate. As we saw in the first part of the presentation we can easily calculate the minimum slew rate, based on the frequency and amplitude of the signal. For a sine wave frequency of 194.4 kHz and a peak amplitude of 0.25 V, the minimum slew rate is 0.3 V/ $\mu$ S.

## Photodiode Amplifier Types:

Two ways to use the diode:

### 1) The Photovoltaic Mode:



Note ground – no voltage across diode

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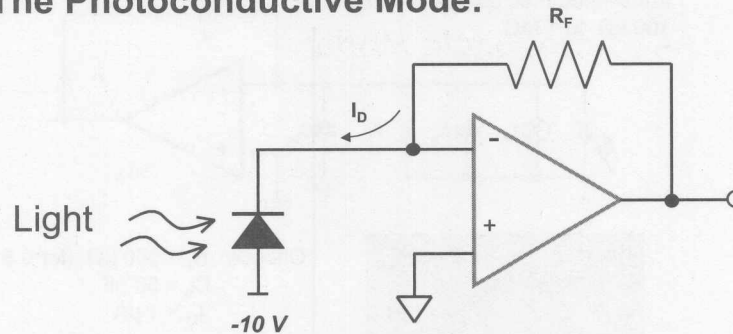
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A photodiode is used as the optical detector in a barcode scanner. The arrangement with an Op-Amp is as shown. When the diode is unbiased as shown, the mode of operation is called photovoltaic mode. In this mode, the capacitance of the diode will be at a maximum. In the analysis of the circuit, we will see that lower capacitance is better for bandwidth and noise reasons.



## Photodiode Amplifier Types:

### 2) The Photoconductive Mode:



-Note - there is voltage across the diode

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In the figure above, a negative bias is provided for the diode detector. This mode of operation is called photoconductive mode. The advantage is a lower capacitance associated with the diode. In this sense, the diode is also a varactor, meaning that the capacitance changes with voltage.

The Op-Amp in the configuration shown is a good choice for this application because it is capable of providing the gain needed and the virtual ground at the inverting input provides an excellent summing junction. An Op-Amp has high input impedance, thus minimizing interaction between the Op-Amp input stage and the diode/ $R_F$  junction.

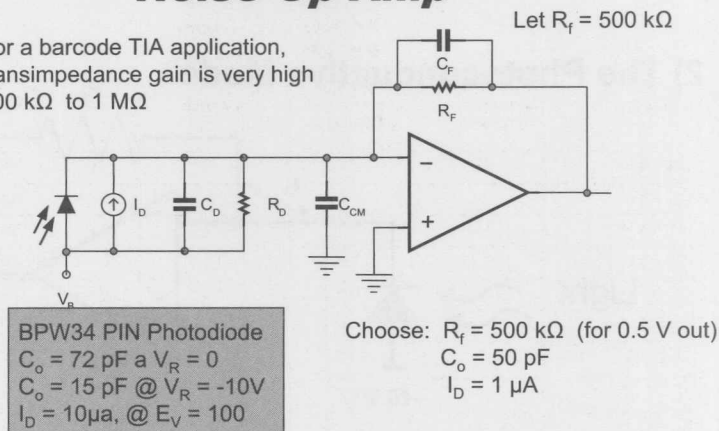
Consequently, the output voltage of this circuit is simply the diode current  $I_D$ , times the feedback resistor. The units of gain for this circuit are simply the transimpedance or  $V_O/I_D$ . The direction of current as shown from the diode causes the Op-Amp output to be positive.

*Back bias  
high - reduce  
capacitance.*



## TIA CIRCUIT High-Frequency, Low-Noise Op-Amp

For a barcode TIA application, transimpedance gain is very high  
100 k $\Omega$  to 1 M $\Omega$



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Shown here is the complete circuit of a single stage solution for the barcode TIA application. A later exhibit will discuss a second possibility for this applications. A full description of the photodiode includes the photodiode current,  $I_D$ , and the photodiode capacitance and resistance,  $C_D$  and  $R_D$  respectively.  $R_D$  turns out to be very high, in the range of 100 megohms.  $C_{CM}$  is the common mode capacitance of the Op-Amp. In the analysis this capacitance will be combined with the diode capacitance. Shown in the box on the left are parameters of a popular PIN Photodiode, BPW34. The characteristics of this device will be used in our example design.

Here are the parametrics to be used in this example.

$$I_D = 1 \mu\text{A}$$

$R_f = 500 \text{ K Ohms}$ . The choice of 500K is driven by the decision to create a circuit with an output of 0.5 V,  $1 \mu\text{A} \times 500 \text{ K} = 0.5 \text{ V}$ .

$C_o = 50 \text{ pF}$ . This corresponds roughly to an unbiased photodiode. Also, 50 pF includes the common mode input capacitance of the Op-Amp,  $C_{cm}$ .

The output voltage in this circuit is merely  $R_f \times I_D$ . This is true under the assumption the input impedance at the inverting input of the Op-Amp is high compared to 500 K Ohms. A MOSFET or JFET input Op-Amp will meet this requirement because of its extremely low input bias current.  $C_f$  is a calculated value, as we will show later, and is necessary for overall stability.

## Choosing Op-Amps

Device	Input Noise Voltage (nV/RtHz)	Input Noise Current (pA/RtHz)	Input Capacitance (pF)	I <sub>bias</sub> (max)	GBWP (MHz)	GBWP/C <sub>in</sub> (MHz/pF)
LMH6628	2	2	1.5	20 $\mu$ A	200	133
LMH6626*	1.0	1.8	0.9	20 $\mu$ A	500	556
LMH6624*	0.92	2.3	0.9	20 $\mu$ A	500	556
LMH6622	1.6	1.5	0.9	10 $\mu$ A	200	222
LMH6654 /6655	4.5	1.7	1.8	12 $\mu$ A	150	83
LMH6672	4.5	1.7	2	14 $\mu$ A	100	50
LF411A	25	0.01	4	200 pA	4	1
LMV751	7	0.005	5	100 pA	5	1
LMC662	22	0.0002	4	0.01 pA (typical)	1.4	0.3
LMV771	8	0.001	4	100 pA	4	1



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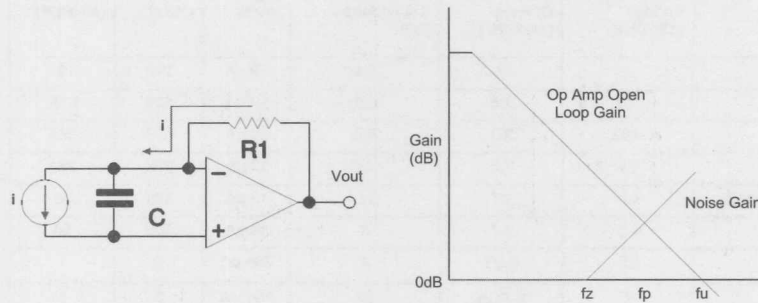


If wide bandwidth is not important,  $C_f$  can be increased to reduce the Op-Amp bandwidth to offset the voltage noise of large feedback resistors, and Op-Amps with low input bias currents will have correspondingly low noise currents.

The table above shows several VFB Op-Amps with high GBW for fast applications. A rough measure of the maximum possible I-V bandwidth is the ratio of  $GBWP/C_{IN}$ . Other Op-Amps with exceptionally low input capacitance and input noise current are more suitable for lower-speed applications with DC accuracy and low noise as the goals.

For high-speed I-V converters the CFB Op-Amp is not generally recommended because the inverting input current noise is higher than that of the non-inverting input. Also the I-V gain is constrained by the size of the feedback resistor used to set the Op-Amp bandwidth (in the range of 500 Ohms to 3 k Ohms). Nevertheless the CFB Op-Amp can play a role in transimpedance converters, as we will see in the following analysis of transimpedance amplifier stability.

# The Transimpedance Amplifier



$$f_z = 1/2 \pi CR1 \text{ where } C = \text{Input capacitance} + \text{Source capacitance}$$



$$f_s = \sqrt{f_z \cdot f_u}$$

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When a transimpedance amplifier is connected to a photodiode, there is a strong chance that the circuit will oscillate unless some compensation in the form of  $C_f$  is provided.

The reasons for this have to do with the capacitance of the signal source, along with parasitic lead capacitance and the input common-mode capacitance of the Op-Amp package that are inevitably present at the inverting input. This capacitance  $C$ , which can be from 1 or 2 pF to over 200 pF, along with the feedback resistor  $R1$ , forms a feedback pole that, closed loop, causes the noise gain to begin to increase at a frequency  $f_z$  in the noise-gain transfer function where

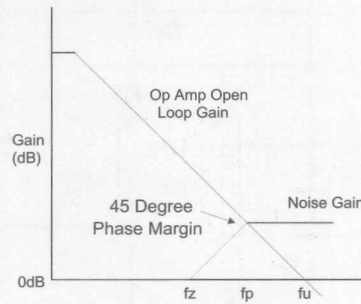
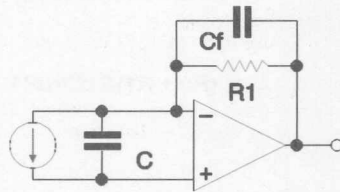
$$f_z = 1/2\pi R1C$$

As this bode plot shows, the resulting zero causes the noise gain to increase at a 6 dB/octave rate above  $f_z$  (and with a 90° phase shift) until it meets the open-loop response (which is falling at a 6 dB/octave rate, also with a 90° phase shift) at frequency  $f_s$ . The net 12 dB/octave rate (net phase shift of 180°) at the frequency of intersection  $f_s$  means there is a very good chance for oscillations to occur.

The frequency  $f_s$  is the geometric mean of  $f_z$  and  $f_u$  and so

$$f_s = \sqrt{f_z \cdot f_u}$$

## Capacitor Compensation



$$C_f = \sqrt{C/2\pi f_u R1}$$



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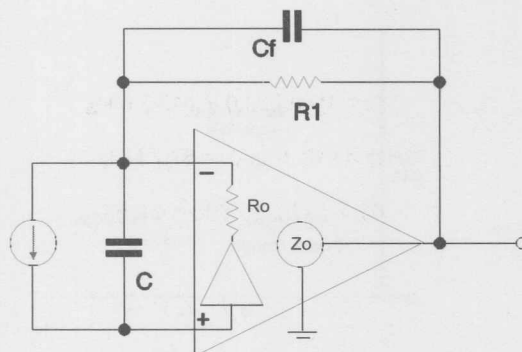


Compensation is achieved simply by placing a small capacitor  $C_f$  across the feedback resistor  $R1$  to form another pole at the frequency  $f_s$ . This introduces a 45° phase shift in the noise-gain response at  $f_s$  ensuring stability.

$$C_f = \sqrt{C/2\pi f_u R1}$$

Larger values for  $C_f$  can be used for even more phase margin, or alternatively, the capacitor can be selected to optimize the pulse response.

## CFB Inverting Input Resistance



$$C_f = (\sqrt{R_1/R_o})(C/2\pi f_u R_1)$$

$$f_z = (R_o + R_1)/2\pi C R_o R_1$$

$$(f_u = f_A = Z_o(f)/R_1)$$

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While the same analysis can be applied to the CFB Op-Amp, the low output impedance  $R_o$  at the inverting input will materially affect the position of the feedback pole, placing it much higher in frequency compared to that for the comparable VFB Op-Amp (with a similar closed loop bandwidth with the chosen value of  $R_1$ ). The size of the compensation factor is reduced by the factor  $\sqrt{R_1/R_o}$

$$C_f = (\sqrt{R_1/R_o})(C/2\pi f_A R_1)$$

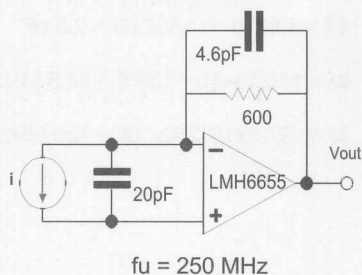
and the frequency at which the noise gain starts to increase is given by

$$f_z = (R_o + R_1)/2\pi C R_o R_1$$

Note that for the CFB Op-Amp, the upper frequency  $f_u$  (now  $f_A$ ) is determined by the size of the feedback resistor  $R_1$  where

$$f_u = f_A = Z_o(f)/R_1$$

## Calculating the Capacitor



$$f_z = 1/2\pi 600 \cdot 20^{-12} = 13.3 \text{ MHz}$$

$$f_s = \sqrt{13.3^6 \cdot 250^6} = 57.7 \text{ MHz}$$

$$C_f = \sqrt{1/2\pi 250^6 600} = 4.6 \text{ pF}$$



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Take the case of a high-speed current DAC presenting a 20 pF load to the transconductance buffer input. With a 250 MHz VFB Op-Amp such as the LMH6655 and a feedback resistor of 600  $\Omega$ , the noise gain starts to increase at frequency  $f_z$  where

$$f_z = 1/2\pi 600 \cdot 20^{-12} = 13.3 \text{ MHz}$$

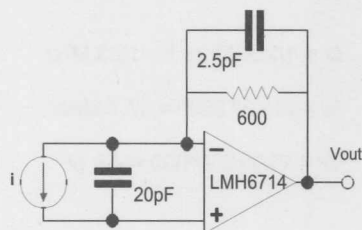
The frequency of intersection of the noise gain with the open-loop gain is

$$f_s = \sqrt{13.3^6 \cdot 250^6} = 57.7 \text{ MHz}$$

The required compensation capacitor is

$$C_f = \sqrt{1/2\pi 250^6 600} = 4.6 \text{ pF}$$

## Calculating the Capacitor



$$f_A = 250 \text{ MHz with } R1 = 600\Omega$$

$$C_f = 4.6 \times 10^{-12} \sqrt{180/600} = 2.5 \text{ pF}$$

$$f_z = 1/2\pi \times 20 \times 10^{-12} \times 138.5 = 57.5 \text{ MHz}$$

$$f_s = \sqrt{57.5 \times 10^6 \times 250 \times 10^6} = 120 \text{ MHz}$$



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With the same feedback resistor of 600  $\Omega$ , the LMH6714 CFB Op-Amp will have a closed loop non-inverting bandwidth of 250 MHz and has an inverting input resistance of 180  $\Omega$ . The compensation capacitor

$$C_f = 4.6 \times 10^{-12} \sqrt{180/600} = 2.5 \text{ pF}$$

The noise gain starts to increase at

$$f_z = 1/2\pi \times 20 \times 10^{-12} \times 138.5 = 57.5 \text{ MHz}$$

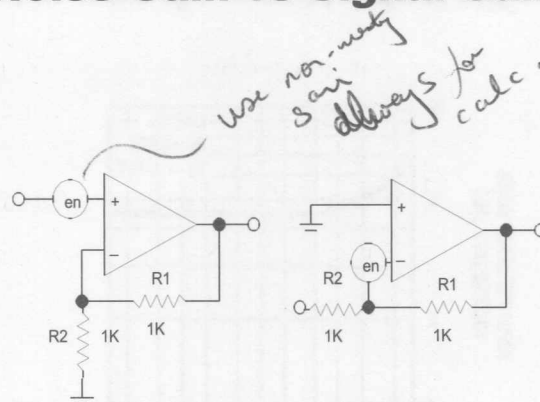
and so the signal bandwidth is

$$f_s = \sqrt{57.5 \times 10^6 \times 250 \times 10^6} = 120 \text{ MHz}$$

Apart from needing a smaller capacitor, the CFB Op-Amp has a wider signal bandwidth than the comparable VFB Op-Amp.

Another advantage of the low CFB Op-Amp inverting input impedance is that DAC switching glitches, which can produce large voltage transients at the input to a VFB Op-Amp, are absorbed, helping improve the settling time.

## Noise Gain vs Signal Gain

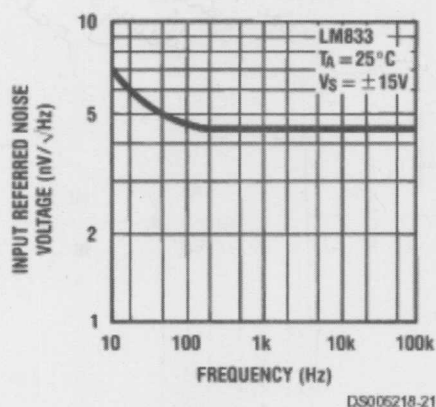


In the previous analysis of the transimpedance amplifier stability, we have referred to the *noise gain* of the amplifier. This is because, in the absence of any signal other than noise, it is the gain to this noise that will determine if the amplifier will oscillate at some higher frequency as the overall phase shift approaches 180°.

In a stable system, the noise generated at the output of the Op-Amp is important, since in most cases the input stage signal to noise ratio (SNR) will dominate the overall SNR of the entire signal path. The noise at the output of the Op-Amp will include noise from the various external passive components and noise from the amplifier's internal passive and active circuits. Since the amplifier gain can be changed by the choice of the external components, the amplifier noise is specified as an equivalent noise generator located at the inputs to the amplifier. This generator can be shown at either the inverting or non-inverting inputs and is usually specified in terms of the noise voltage in a bandwidth of 1 Hz. We are neglecting current noise for the moment.



## Op Amp Noise Spectrum



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A typical noise voltage spectrum of an Op-Amp such as the LM833 designed for low noise, medium frequency applications looks like this. The broadband noise is low, less than 5 nV/√Hz, (for general purpose Op-Amps this can be at least a factor of 10 higher) but exhibits an increasing level at low frequencies.

The noise of an Op-Amp increases from the broadband noise level as the frequency approaches DC. The low frequency noise is known as 1/f noise and is important in DC and precision applications. For high-speed applications the 1/f noise usually can be ignored.

## Noise Voltage

Bipolar:

$$e_n = \sqrt{4kT(r_b + 26 \text{ mV}/2I_c)}$$

*input stage current*

MOSFet:

$$e_n \approx \sqrt[4]{\text{AREA}}$$

*α area  
area ↑ noise ↓*



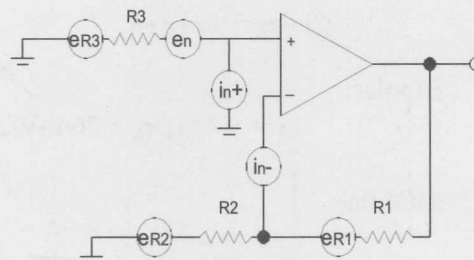
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The broadband noise voltage depends on a number of factors. For a bipolar design the noise voltage depends in part on the size of the resistance between the input terminal and the actual base-emitter junction, which can be minimized by increasing the device size and paying careful attention to layout. When extremely low noise design is required this extrinsic base resistance noise can be the limiting factor, but most of the time, the second term showing that the noise depends on the inverse of the stage transconductance, is dominant. Therefore, to reduce the noise in half the input stage current must increase a factor of 4. CFB Op Amps often run high input-stage currents compared to VFB Op Amps and will have noise voltages in the 2 nV/√Hz 5 nV/√Hz range. The higher input noise current resulting from the higher bias currents are not too significant because the external resistors in which these noise currents flow are usually less than 1 kohm.

For a CMOS or BiFET amplifier, the noise voltage is proportional to the fourth power of the device area, and to cut the noise in half, the area must be increased by a factor of 16. The stage current will also go up by a factor of 16. On the other hand, MOS devices are usually designed for low-power applications and noise current in large external resistors becomes more important.

## Complete Noise Model



$$E_n = \sqrt{NBW} \times \sqrt{(i_{n+}^2 R_1^2 + i_{n+}^2 R_3^2 [1 + R_1/R_2]^2 + e_n^2 [1 + R_1/R_2]^2 + 4kTR_1 + 4kTR_2 [1 + R_1/R_2]^2 + 4KTR_3 [1 + R_1/R_2]^2)}$$



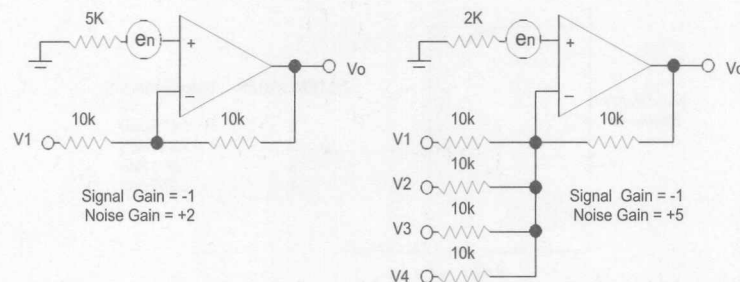
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The complete noise model for the Op-Amp is shown above. Not only is it complex, but the contribution of each source to the total output noise results a large number of terms. Each term is considered to be uncorrelated to any other term, and the total noise is the root of the sum of the squares of each individual noise voltage. Because of this RSS addition, not all terms are equal. For example, if the contribution of any noise source is less than 20% of the contribution of any other noise source, then its contribution to the system noise will be less than 2% of the total. In fact noise sources less than 30% of the largest noise source can probably be neglected.

Each white noise source is increased at the output by the closed-loop non-inverting gain of the amplifier (otherwise known as the noise gain), except for the noise in R2, which is multiplied by the inverting gain, and the noise in R1 and the inverting input current noise in R1, which is applied directly to the output (a gain of 1).

## Noise Gain vs Signal Gain

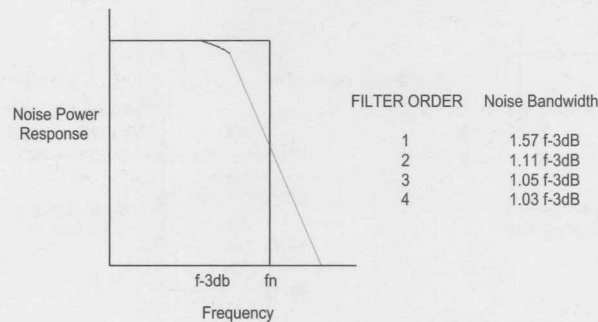


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This shows how important it is to distinguish between signal gain and noise gain. For low gain amplifiers, the difference in inverting and non-inverting gain is large, and in the case of the inverting summer it can become very large indeed. Using the wrong gain can result in significant errors.

## Noise Bandwidth



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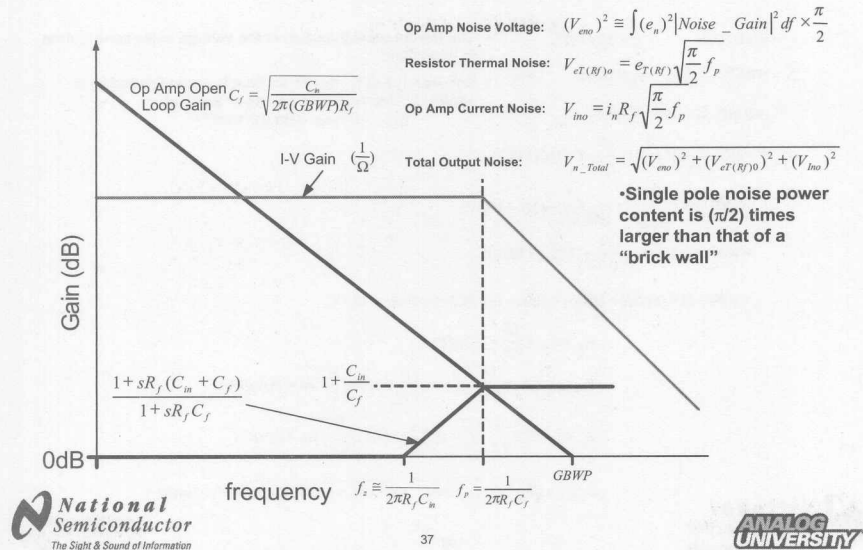
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Another easy mistake to make in calculating the total noise is to assume the bandwidth is the signal bandwidth. In noise calculations, a noise power bandwidth is used and this has a 'brick-wall' filter response. The maximum power gain of the transfer function  $T(j\omega)$  multiplied by the noise bandwidth must equal the total noise that passes through the transfer function.

For a response with a single RC roll-off, the noise bandwidth is  $\pi/2 f_{-3dB}$ .

If the overall response is not flat and there is high frequency peaking, this also has to be taken into account. Going back to the example of the current to voltage converter will show how all these factors are taken into account.

## Noise Calculations (1)



When analyzing the noise at the output of the I-V converter, it is important to note that the various noise sources (i.e. Op-Amp noise voltage, feedback resistor thermal noise, input noise current, etc.) do not all operate the same frequency band. The Op-Amp noise voltage will be gained up in the region between the noise gain's "zero" and its "pole". The higher the value of  $R_f$  and  $C_{in}$ , the sooner the noise gain peaking starts and the larger its contribution would be to the total output noise. Therefore, it's obvious to note that it is advantageous to minimize  $C_{in}$  (e.g. by proper choice of op amp, by applying a reverse bias across the diode at the expense of excess dark current and noise). Unfortunately, most low-noise op amps have a higher input capacitance compared to ordinary ones.

The " $\pi/2$ " factor within the square root will account for the single pole response.

For the Op-Amp noise voltage, the calculation is slightly more complicated since the total noise contribution would involve an integration as the noise gain varies with frequency.

## Noise Calculation (2)

$$e_n = 10 \text{ nV} / \sqrt{\text{Hz}}$$

$$i_n = 3 \text{ pA} / \sqrt{\text{Hz}}$$

$$f_z = 100 \text{ KHz}$$

$$f_p = 1 \text{ MHz}$$

$$C_n = 50 \text{ pF}, C_f = 5 \text{ pF}, R_f = 32 \text{ K}$$

• The low frequency portion of the voltage noise contribution is negligible

• Between  $f_z$  and  $f_p$ , the Noise Gain is approximated by a +20dB/decade response having a "zero" at  $f_z$ : [Noise Gain (f)]<sup>2</sup> = 1 + f<sup>2</sup> / f<sub>z</sub><sup>2</sup>

$$(V_{en})^2 = [10(\frac{nV}{\sqrt{\text{Hz}}})]^2 \cdot \int_{f_z}^{f_p} (1 + \frac{f^2}{f_z^2}) df + 100(\text{KHz})$$

$$= 100e - 18 \cdot \int_{100 \text{ KHz}}^{1 \text{ MHz}} (1 + \frac{f^2}{(100 \text{ KHz})^2}) df + 100e3$$

$$= 100e - 18 \cdot \{ [f + \frac{f^3}{3 \times (10e9)}]_{100 \text{ KHz}}^{1 \text{ MHz}} + 100e3 \}$$

$$= 100e - 18 \times \{ 34.2e6 + 100e3 \} \approx 100e - 18 \times 34.2e6 = 3.43e - 9 (V^2)$$

$$V_{en} = V_{en} \cdot \sqrt{\frac{\pi}{2}} = 73.4 (\mu V)$$

$$V_{et(RF)} = e_{t(RF)} \times \sqrt{\frac{\pi}{2}} \times f_p = 4(\frac{nV}{\sqrt{\text{Hz}}}) \times \sqrt{32} \times \sqrt{\frac{\pi}{2}} \times 1e6 = 28.4 (\mu V)$$

$$V_{no} = i_n \times R_f \times \sqrt{\frac{\pi}{2}} \times f_p = 3(\frac{pA}{\sqrt{\text{Hz}}}) \times (32e3) \times \sqrt{\frac{\pi}{2}} \times 1e6 = 120 (\mu V)$$

$$V_{n\_Total} = \sqrt{V_{en}^2 + V_{et(RF)}^2 + V_{no}^2} = \sqrt{(73.4)^2 + (28.4)^2 + (120)^2} (\mu V) = 144 (\mu V)$$



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Here are the calculations based on an example to show how the noise is integrated over the noise gain. The noise gain is assumed to have a single zero at 100 kHz and the pole at 1 MHz is ignored for simplicity. The noise density (nV/√Hz) function is multiplied by the noise gain magnitude and then squared before being integrated over the total range (0 Hz to 1 MHz).

The other simplifying assumption made is that the op amp noise voltage is constant over the entire range. This is not a bad assumption since the contribution of the 1/f region of the op amp is negligible in a situation like this where BW reaches into the MHz region.

As far as the input noise current ( $i_n$ ) is concerned, there is only a single pole located at  $f_p$ . The same is true for the RF noise voltage which sees a single roll-off at  $f_p$ .

The resultant noise voltage from all sources is then summed together in a square root of the sum of the squares fashion before arriving at the total rms output noise (V).

It turns out that the dominant noise source would be the op amp input noise current. The op amp input noise current is given by:  $\sqrt{(2qI_b)}$ , where  $I_b$  is the input bias current. Therefore, it's obvious that choosing a device with minimal input bias current would be advantageous in terms of noise.





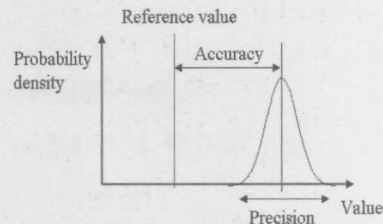
## **Precision Amplifiers and Sensor Interfacing**

**The Need for Precision**



## What is Precision?

- **Definitions:**
  - Accuracy
  - Precision
- **Difference between precision and accuracy**
- **Cannot have accuracy without precision!**



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In science and industry, accuracy is the degree of conformity of a measured or calculated quantity to its actual, nominal, or some other reference value. Precision characterizes the degree of mutual agreement among a series of individual measurements, values, or results.

The difference between the two: repeated measurements are compared to arrows that are fired at a target. Accuracy describes the closeness of arrows to the gold at the target center. Precision would be the size of the arrow cluster. When all arrows are grouped tightly together, the cluster is considered precise since they all struck close to the same point, if not necessarily near the gold.

We cannot have accuracy without precision, but it is possible to have it the other way around. Remember that all arrows could be clustered (precision) without being close to the gold, but if all arrows are not clustered (no precision), then you cannot possibly have accuracy. The goal is to have measurement devices that are both accurate and precise.

## **What is Precision?**

- **Precision amplifiers:**
  - **Untrimmed:**  $V_{os}$  less than or equal 1 mV
  - **Trimmed:**  $V_{os}$  between 100  $\mu$ V and 1 mV
  - **Special techniques:**  $V_{os}$  less than or equal to 100  $\mu$ V
    - **Special techniques:**
      - **Composite amplifier**
      - **Chopping action**



3



What has been the accepted definition of precision amplifiers depends heavily on the offset voltage. If the Op-Amp can achieve an offset voltage of 1 mV or below without using any trim techniques, the Op-Amp is considered to be precision. If laser trim has been used in the amplifier, then the offset voltage needs to be less than 1 mV and can usually go down to as low as 100  $\mu$ V. Usually for achieving offset voltages less than that, special techniques are required. These special techniques include use of chopping action and/or composite amplifiers.

## **Offset Voltage and Drift**

- **Definition of offset voltage**
  - Usually modeled as a voltage source on the non-inverting input
- **Definition of offset voltage drift**
  - Also known as offset voltage error



4



Offset voltage is one of the many characteristics of a “non-ideal” Op-Amp. For an ideal Op-Amp, the output voltage sits at mid-supply when there is no differential voltage applied between the inputs of an Op-Amp. However, in reality, the output will be away from mid-supply value by a minimal amount. To correct this, a small amount of differential voltage needs to be applied between the inputs of the amplifier. The amount of differential voltage required to bring the output back to mid-supply is referred to as “input offset voltage” or simply “offset voltage.”

Another way of looking at this: when there is no external differential voltage applied between the input of the amplifier, a small amount of voltage present in the circuit will be gained up by the amplifier’s gain and will show up on the output. So, if the amount of “output offset voltage” is known, we can calculate the input offset voltage using this relationship:

$$\text{Input offset voltage} = (\text{output offset voltage}) / (\text{Op-Amp's closed loop gain})$$

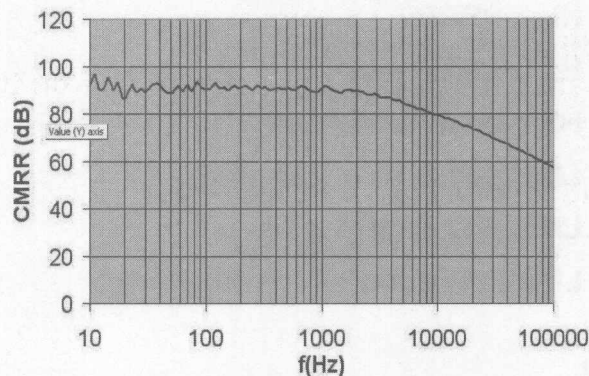
The value of offset voltage changes under different conditions, or “drifts” The two main elements contributing to this drift are passing of time and change in temperature. However the time factor is less important and the term offset “voltage drift” usually refers to the temperature component.

For general purpose Op-Amps, this value is not very important since it is usually orders of magnitude smaller than the actual offset voltage. In precision amplifiers, this value is of special importance since it could very well cause the offset voltage to double or triple at temperature extremes.

Input offset drift over time is the change in offset voltage per year (or another specified time frame).

## CMRR

CMRR VS frequency



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Op-Amps are designed so that they will only respond to a differential voltage between the two input pins. This means that for an ideal Op-Amp, if the same voltage is applied to both input pins, the output will remain unchanged. This is referred to as the “common-mode” signal. For an ideal Op-Amp, the “common-mode” signal does not change the output at all, meaning the Op-Amp completely rejects this common mode signal. The ability of an Op-Amp to reject this common-mode signal is shown by the ratio of the common-mode signal seen on the output to the ratio of the common-mode signal on the input and is called “common mode rejection ratio” or CMRR. An ideal Op-Amp has a CMRR of infinity. Real Op-Amps have finite CMRR values which are usually expressed in dBs.

$$\text{CMRR} = 20\log[(\text{Change in offset voltage})/(\text{change in common mode voltage})]$$

or equally:

$$\text{CMRR} = 20\log[(\text{differential gain of amplifier})/(\text{common mode gain of amplifier})]$$

AC CMRR and DC CMRR: whenever there is a reference to CMRR, we are talking about “DC CMRR” or the ratio of differential gain to common-mode gain at zero frequency. The fact is that CMRR is heavily frequency dependent. As we know, the differential gain of an amplifier is relatively frequency independent and remains somewhat the same over a frequency range (it decreases a bit), while the common-mode gain of an amplifier increases with frequency (not a good thing). This means CMRR decreases over frequency.

## Precision Op-Amps

- Low noise at low frequencies (1/f)
- Low Vos and low drift with time and temperature
- High PSRR
- High CMRR
- High open loop gain
- LMP2011 A new standard
- LMP2012 dual
- LMP2014 quad



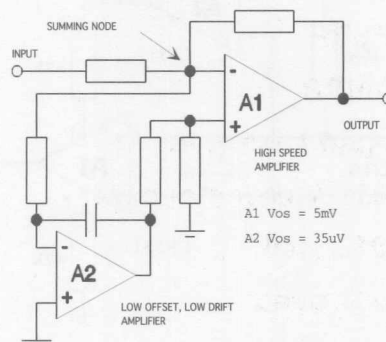
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What makes a precision Op-Amp? Primarily high DC open-loop gain combined with low input offset voltages and offset bias currents. In particular the offsets should not drift with temperature changes or over a period of time. Although the conventional Op-Amp has improved characteristics over many years of development, to the point that many precision applications can be satisfied quite easily, some of the more demanding applications have required a *stabilized* Op-Amp, where special circuit techniques are used to minimize offsets and eliminate the drift in characteristics that occur at initial turn-on and over a long period of continuous operation. In the search for precision, many approaches to *stabilization* have been taken, starting with chopper amplifiers (dating back to vacuum tube days), chopper-stabilized amplifiers, auto-zero amplifiers (with and without sample-and-holds), composite amplifiers, and combinations of all of the above. In fact, it can sometimes prove difficult to establish, from the name alone, exactly how the stabilization is being achieved.

Since nearly all *stabilized* amplifiers (with the possible exception of the basic chopper amplifier) are actually composite amplifiers, ie a combination of two amplifiers with different characteristics, we will start with this in describing how the LMP201X works.

## The Composite Amplifier



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In the case of the precision Op-Amp, wide bandwidth is frequently sacrificed to obtain good performance at or close to DC. Nevertheless, some precision applications require high closed-loop gain along with a reasonable closed-loop bandwidth. A 1 MHz GBW may seem to be pretty impressive, but with a closed loop (signal gain) of 40 dB, the closed-loop bandwidth is only 10 kHz, and for low distortion, the signal bandwidth is much less, closer to 1 kHz!

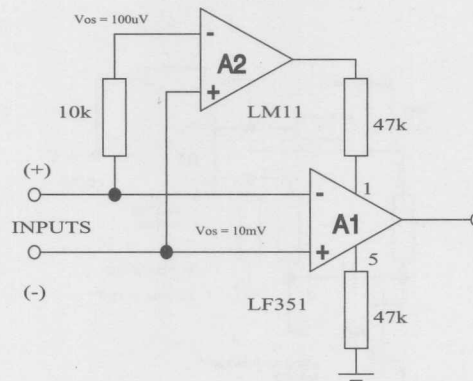
High GBW amplifiers are available ( $\geq 5$  MHz), but, for unity-gain stability, these usually have lower DC open-loop gain ( $\leq 110$  dB) than would be suitable for precision applications and have offsets that are an order of magnitude too high ( $\geq 1$  mV).

The composite amplifier resolves this dilemma by connecting two amplifiers in parallel across the signal input. A1 is a high-speed amplifier with modest DC characteristics. A2 is a low-speed amplifier with low input offsets and low drift.

For A1 alone, with the non-inverting input connected to ground, for zero signal input the output should be at ground potential, and hence the inverting input will be at ground. This is the ideal case when there are no offsets. However, if A1 has an input offset voltage of 5 mV, the output will have to move to put the inverting input 5 mV away from the non-inverting input. With a closed-loop gain of 40 dB, the output then has to move 500 mV away from ground instead of remaining at zero. In the composite amplifier, A2 inverting input is also connected to the summing node, with its non-inverting input connected to ground. However, the offset voltage for A2 is only 35  $\mu$ V, and if the output of the composite amplifier moves the summing node more than 35  $\mu$ V away from ground potential, this difference, multiplied by the dc open loop gain of A2, will appear at the output of A2 and be applied the non-inverting input of A1. In essence then, the output of the composite amp will only move far enough to put the summing junction 35  $\mu$ V away from ground. With a closed loop gain of 40 dB, this is only 3.5 mV compared to the 500 mV for A1 alone.

There are several clear-and not so clear-disadvantages to this stabilization technique. The offset is still not reduced to zero and can still drift with time and temperature (dependent on the offset and drift characteristics of A1). Since the non-inverting input of A1 is used to provide the correction signal, the composite amplifier can be used only in the inverting mode.

## Full Differential Input



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By using the high-speed amplifier compensation pin, this composite amplifier has a full differential input. This is shown in Fig 5-24 of Frederiksen's book *Intuitive Operational Amplifiers*, where the composite amplifier is comprised of an LM11 (input offset current 0.5 pA, input offset voltage 100  $\mu$ V, long term stability 10  $\mu$ V/year) and an LF351 (GBW 4 MHz, input offset 10 mV).



## Precision Specifications

- **Vos** 0.8  $\mu\text{V}$
- **Vos Drift** 0.015  $\mu\text{V}/^\circ\text{C}$  over temperature  
0.006  $\mu\text{V}/\text{month}$  over time  
2.5  $\mu\text{V}$  over life
- **CMRR** 130 dB
- **PSRR** 120 dB
- **Avol** 130 dB
- **Fast settling** 1.4  $\mu\text{S}$  to 0.01% large signal
- **Overload recovery** 40 mS (no large external capacitors)

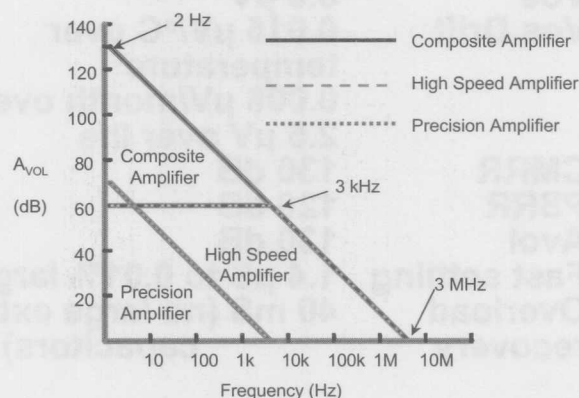


This summarizes many of the excellent precision characteristics of the Op Amp.

Often overlooked are inadvertent thermocouple problems that can produce offset errors with temperature far in excess of the Op-Amp itself. Kovar, a common lead frame material used for integrated circuits, will produce errors of more than 35  $\mu\text{V}/^\circ\text{C}$  when soldered into a copper printed circuit board. A temperature difference of only 0.0014  $^\circ\text{C}$  between the board and the lead will introduce thermocouple noise equal to that of the LMP201X. The LMP201X series uses a copper lead frame.

Because there are no large external capacitors to store the unadjusted offset voltage (common to many stabilized amplifiers), recovery from overdrive takes less than 40 mS compared to 250 mS to several seconds for other amplifier types.

## Open-Loop Response



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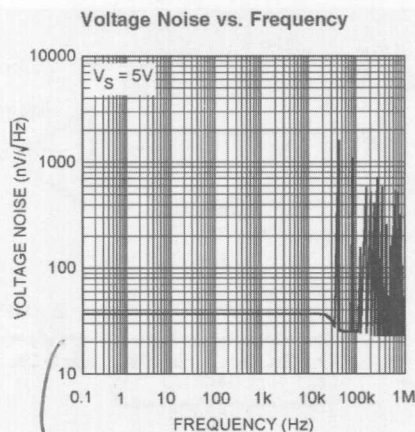
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A not so obvious problem with composite amplifiers is matching the frequency/gain responses of the two amplifiers to produce a smooth overall response. In the LMP2011, both amplifiers are fabricated on the same die, producing excellent matching as shown here.

Each amplifier has a single dominant pole so the AC gain for both falls at a -6 dB/octave rate. The corner frequency for the high-speed amplifier is set at 3 kHz (dashed line), whereas for the low-speed amplifier this pole frequency is at 2 Hz (dotted line). The  $g_{ms}$ ' of the two amplifiers are also matched to produce a pole/zero cancellation, i.e. the open-loop gain of the low frequency amp falls to 0 dB at the same frequency as the high-frequency amplifier pole frequency (6 kHz). This produces the smooth overall response of the composite amplifier shown as a solid line. The AC gain falls at a -6 dB/octave rate through the entire useable frequency range. The combined open-loop gain is 130 dB, well within the range for precision applications and the 3 MHz unity-gain crossover frequency allows wide signal bandwidths at high closed-loop gain.

A large gain bandwidth product and a wide output stage bandwidth is important for rapid recovery from load transients caused by ADCs or multiplexers.

## No 1/f Noise



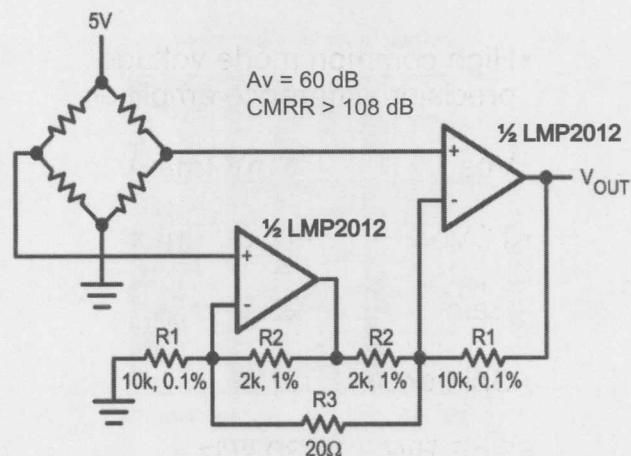
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Low frequency noise is treated as a slowly moving DC offset and is therefore zeroed out by the LMP2011. This produces the noise spectrum shown above, where the noise voltage is flat down to DC and there is no 1/f corner frequency. The broadband noise is higher than for many low noise Op-Amps because the low frequency noise components are being averaged across the entire frequency range (a spread spectrum effect).

In DC or very low-frequency measurement systems, this lack of 1/f noise can be very important. Take a conventional amplifier with a flat-band noise voltage of 10 nV/√Hz and a noise corner frequency of 10 Hz. The RMS noise at 0.001 Hz is going to be 1 μV/√Hz and at a gain of 1000 will represent an error of 0.5 mV(p-p) in the frequency range 0.001 Hz to 1 Hz. The output error of the LMP2011 is only 0.21 mV over the same frequency range.

## Precision Strain Gauge



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A good example of a precision application is the strain gauge. Here the LMP2012 Op-Amp is used to raise the signal level by 60 dB with low offset and low drift over temperature and time. The worst case CMRR of 108 dB is set by the resistor matching of 0.1%. Tighter tolerance or trimming would improve the CMRR if needed.

## LMP8270

- High common mode voltage precision difference amplifier

- Vos 1 mV (max)
- TC Vos 15  $\mu$ V (max)
- Gain 20 V/V
- Gain error 0.1%
- 3 dB BW 80 kHz

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• CMVR

-2 V to +27 V

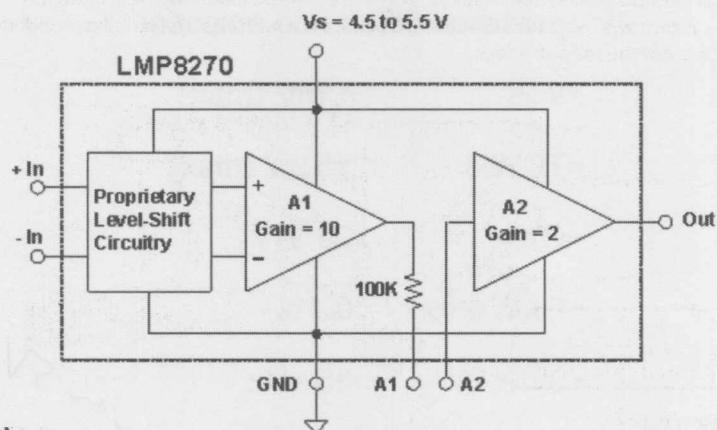
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In some applications, there is not only a need for precision, but also for the ability to withstand voltage sources that are outside the supply voltage range of the Op-Amp. In automotive applications, the ground potential of a sensor (chassis ground) may be several volts different from the ground potential back at the microprocessor. Load dump (loss of battery) or double-battery jump-starting can produce source voltages more than double the normal supply voltage.

The LMP8270 is a high common-mode voltage difference amplifier that amplifies differential voltages at extremely high common-mode voltages (fully functional up to 27 volts, with reduced accuracy up to 40 V under a load dump) while operating from a 5 V supply.

## LMP8270: Block Diagram



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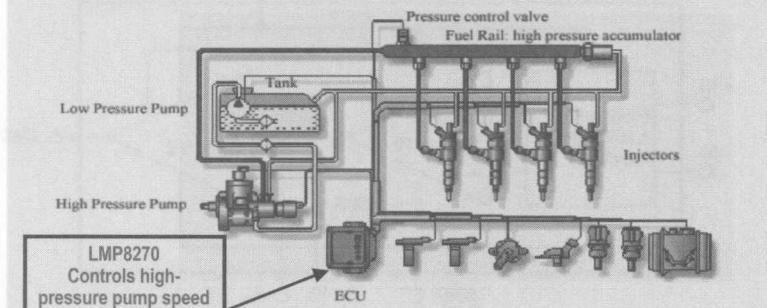
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The fixed gain of 20 is achieved with two gain stages. Filters may be connected between the stages.

## System Architecture: Diesel Injection Control

### Common Rail system

Common Rail systems allow to integrate the Diesel engine's injection system with various remote functions while enhancing flexibility in defining the combustion process.



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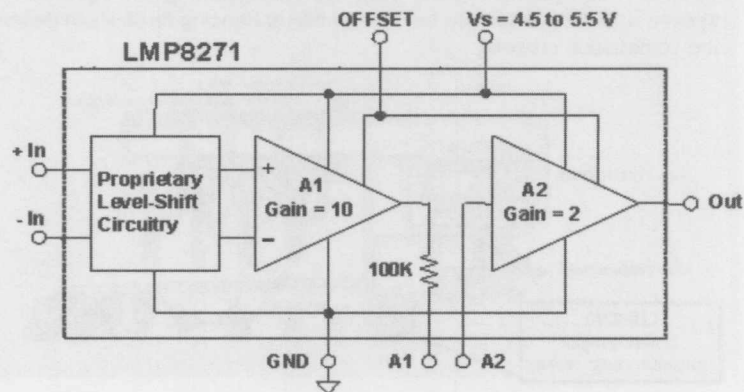
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Here is an example of the LMP8270 in a common rail system. Since the control unit may be relatively remote from the engine peripherals, the high common-mode input range of the LMP8270 is critical for ensuring high performance.



## LMP8271

- Very similar to LMP8270
- Has an offset adjustment pin



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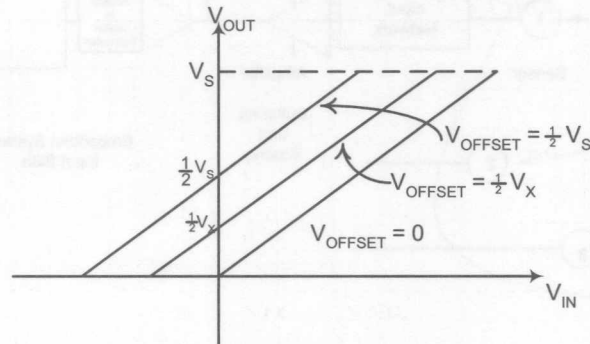
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For most current-sensing applications, the Op-Amp is amplifying the voltage across a sense resistor. This voltage is caused by a uni-directional current flow in the resistor. In some circumstances, the current may flow in either direction. The LMP8271 is able to accommodate a bi-directional current flow with an external offset adjustment pin.

## LMP8271: Offset Adjustment Pin

### • Mid-rail offset adjustment pin



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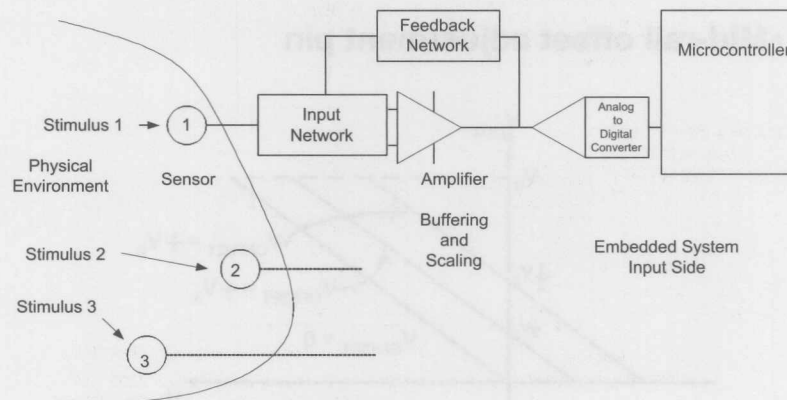
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The external mid-rail offset adjustment pin enables the designer to use this device for bi-directional current sensing. If the offset pin, pin 7, is connected to ground, then the LMP8271 is capable of sensing positive signals. When the offset pin is connected to  $V_S$ , then  $\frac{1}{2} V_S$  is added to the output and under this condition the amplifier can sense both positive and negative signals. If this offset pin is connected to any voltage between ground and  $V_S$ , then the output is increased by a voltage equal to half of that offset, e.g. if the offset is connected to  $V_X$ , then the output increases by  $\frac{1}{2} V_X$ . The figure shows how this works.

Note that the offset pin, pin 7, needs to be connected at all times. If the pin is left floating, the LMP8271 will be operating in an undefined mode. Also, pin 7 should be driven from a low-impedance source.

# Physical Measurement System



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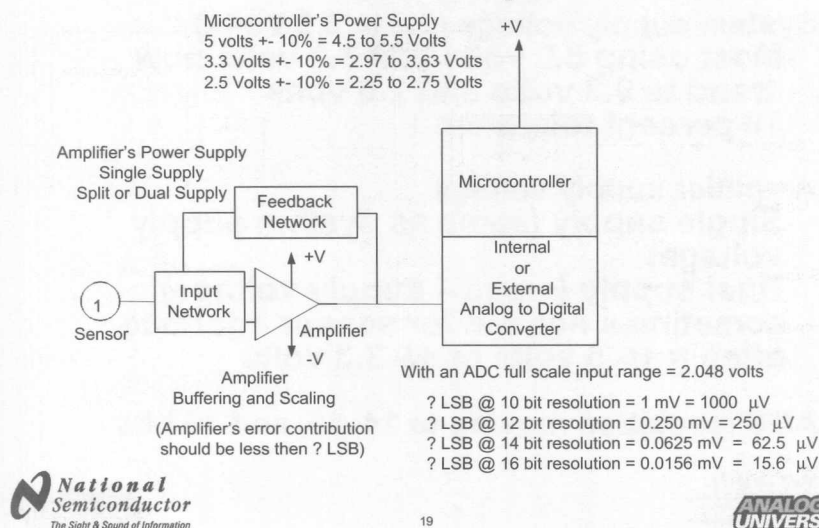
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All control systems require some input from the physical world, which is an analog environment, and sensors frequently provide that input.

Sensors provide the interface from the physical environment to the electrical environment by converting the stimulus of interest into a voltage or current. The output of most sensors is not usable without additional buffering and scaling, which is the function of the amplifier and its input and feedback networks.

## Typical Embedded System Input



Many of the microcontrollers used in embedded control systems are being forced to lower supply voltages as semiconductor processes are migrating to smaller geometries. Digital logic supply voltages have decreased from 5 volts to 3.3 volts and now to 2.5 volts. Some are in the process of migrating to 1.8 volts and even lower.

Amplifier supply voltages are following a similar trend. Recent analog semiconductor processes, (such as National's VIP10®) are able to work on these supply voltages because of the smaller transistor geometries and significant reductions in parasitic diode capacitance. The lower supply voltages also reduce the dynamic range available for amplifiers and ADCs. At the same time the required resolution of the signal processing path is increasing.

A short time ago, a 12- to 14-bit ADC with a 10 volts full-scale input was considered good. Now, 16 bits and higher are expected with full-scale inputs of 1 to 2 volts. This results in error budgets in the several tens of microvolt range.

## **Market Trends**

- **System supply voltage (2.2 to 5.5 Volts)**
  - Most using 5.0 volts and 3.3 volts now trend to 3.3 volts and 2.5 volts
  - 10 percent tolerance
- **Amplifier supply voltage**
  - Single supply (same as system supply voltage)
  - Dual supply (+ and – supply voltage) sometimes needed for sensor interface, often = +/- 5 volts or +/- 3.3 volts
- **ADC resolution moving to 14, 16, and 18 bits**



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Amplifying the sensor's output is often thought of as the primary function of the amplifier, but the sensor's output characteristics and the ADC's input characteristics also have a significant effect on the total system precision.

On the input side, each type of sensor has a unique set of parameters that must be accounted for. Characteristics such as source impedance, signal level, dynamic range, etc. are part of the design constraints for the input and feedback network of the amplifier.

On the output side, the input characteristics of the ADC will effect the loading on the output of the amplifier. Most of the new ADCs have a switched capacitor input which presents a dynamic reactive load to the amplifier.

## ***The Amplifier's Roles***

- **Accurately scale the sensor's signal**
- **The amplifier must provide a suitable interface to the sensor dependent on the sensor's characteristics including source impedance and sensitivity**
- **Dynamic range interface to the ADC, what type of load is presented by the ADC?**
  - **Resistive**
  - **Switched capacitor**



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The primary tasks that the amplifier performs are scaling the signal, avoid loading the sensor output, and being able to drive the full-scale input of the ADC.

## ***Interfacing the Sensor to the ADC***

- **The amplifier may be needed to reduce error sources**
  - **Remove any common mode components**
  - **Remove offsets inherent in the sensor's output**



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In cases where the probe is remote from the amplifier input, the amplifier has to withstand any common-mode voltages that may be present (see previous section on the LMP8270). Some sensors will have inherent offset voltages requiring correction so that the ADC can operate with the maximum dynamic range.



## ***The Amplifier's Requirements***

- Precision sensor interface requirements
  - High open-loop gain
  - Low maximum offset voltage
    - Low offset voltage drift
  - Low noise
    - Voltage noise
    - Current noise
  - Low input bias current
  - High common-mode voltage rejection ratio (CMRR)
  - High power supply rejection ratio (PSRR)
  - Bandwidth (appropriate for the signal frequency)  
***Effective signal bandwidth is a function of the amplifier's gain bandwidth, closed-loop gain, AND the measurement system resolution***



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The amplifier's characteristics will set the baseline for how much precision can be archived.

The open loop gain is a factor in the closed-loop gain error and should be as high as possible.

Offset voltage and offset voltage drift are multiplied by the noise gain of the feedback network and should be as low as possible.

The noise voltage and noise current should be small compared to the sensor's signal.

The input bias current should be low relative to the source impedances of the sensor and feedback networks.

Several types of sensors have a common-mode voltage associated with the sensor output which must be removed by the amplifier. The common-mode rejection ratio, CMRR, should be as high as possible.

The power supply may be shared with active digital loads that will generate noise and ripple on power supply distribution circuit. The power supply rejection ratio, PSRR, should be as high as possible.

The amplifier's bandwidth must be calculated based on the precision required for the signal and this is a function of the gain bandwidth and the closed-loop gain. The effective available bandwidth drops rapidly as the required precision increases.

## Op-Amp Error Sources

$$e_{id} = \frac{e_o}{A_{VOL}} + V_{OS} + (I_{B+})(R_{S+}) + (I_{B-})(R_{S-}) + \frac{e_{CM}}{CMRR}$$

- Major input referred error sources of an Op-Amp  
 $e_{id} = 0$  for ideal Op-Amp
- Precision requires error terms required to be small relative to the signal being processed
- $A_{VOL}$  and CMRR are frequency dependent



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This equation considers four of the major contributors to errors in Op-Amps. The value " $e_{id}$ " is the voltage between the two inputs of the Op-Amp and is equal to zero if the Op-Amp is ideal.

The first term,  $e_o/A_{VOL}$ , results from the finite gain of the amplifier. There must be a small differential voltage across the input to produce an output voltage. For example, if the output of an amplifier is 1 volt DC and the open loop gain is 100 dB, the error voltage across the inputs is  $1/105 = 10$  mV.

The second term, input offset voltage or  $V_{OS}$ , is a result of small imbalances in the differential input stage of the amplifier. The input offset voltage is multiplied to the amplifier output by the noise gain of the amplifier. At high gains the  $V_{OS}$  can become a large offset error.

The third and fourth terms result from the input bias currents in conjunction with any source resistance. Any current flowing into the amplifier's input will cause a voltage drop across the source resistance of  $(I_B \times R_S)$ . This has two effects. The first is to generate an apparent offset voltage at the input to the Op-Amp if the equivalent source impedances on each input are not equal. The second is to add an error voltage to the signal that changes its apparent magnitude.

The last term brings in the effect of the common-mode voltage seen by the amplifier's input. The common-mode voltage,  $e_{CM}$ , is defined as the average voltage on the amplifier's inputs,  $(e+ + e-)/2$ . For example, if the common-mode voltage is 1 volt and the CMRR is 80 dB, the error on the amplifier's input due to the common-mode voltage is  $1/104 = 100$  mV.

Each of the above error sources needs to be evaluated with respect to the specifications of the amplifier being considered.

As the frequency of the signal increases, the open-loop gain  $A_{VOL}$  and the CMRR will fall.

## ***The Sensor's Role***

- **Convert a physical phenomena into a voltage or a current**
  - Temperature
  - Force
  - Pressure
  - Position
  - Velocity
  - Acceleration
  - pH
  - Magnetic field
  - Light intensity
  - Radiation
  - etc.



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In the context of this presentation, a sensor makes use of a dependency between the physical measurement of interest and of an electrical property of the sensor such as a change in voltage, current, or resistance.

For example:

A thermocouple's output voltage will change as the temperature difference between the hot junction and cold junction changes.

The resistance of a RTD (Resistance Temperature Detector) changes as the temperature of the resistive element changes.

Most of these types of dependencies have been exploited to create sensors.

## ***Sensor Characteristics***

- **Active or passive**
- **Voltage or current output**
- **Source impedance**
- **Sensitivity**
- **Linearity**
- **Dynamic range**
- **Frequency response**
- **Common-mode signal components**



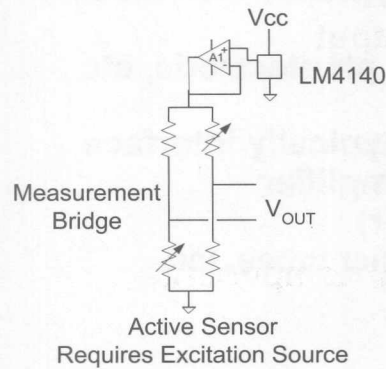
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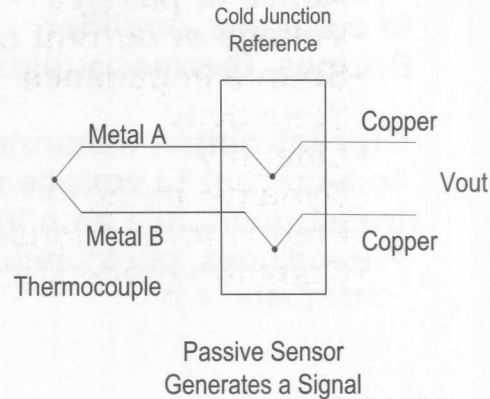
Any sensor will have a set of characteristics that will determine its suitability for a specific application. This list of eight characteristics are common and will be discussed in the following next.

## Active and Passive Sensors

Active sensors will require additional circuitry to drive the sensor elements



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The first important characteristic to know is whether the sensor is active or passive?

The active sensor requires an excitation source in order to generate an output signal. The resistive measurement bridge senses force by changing the resistance of one or more of the bridge's elements. The bridge is driven with a constant current source or a constant voltage source, and the output is a voltage related to the amount of force the sensor is being exposed to.

The passive sensor generates an output signal directly. The thermocouple will generate a voltage based on the temperature difference between the hot junction and the cold junction.

## ***Voltage or Current Output***

- **Voltage-output sensors typically interface to a voltage amplifier**  
**Bridges, thermocouples, pH electrode, etc**
- **Current-output sensors typically interface to a current to voltage amplifier (transimpedance amplifier)**  
**Photodiodes, photomultiplier tubes, Ion chambers, etc**



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The voltage-output sensor and the current-output sensor will have different amplifier topologies. Typically, the voltage-output sensor will use a voltage amplifier while the current-output sensor uses a transimpedance amplifier to convert the current to a voltage.

## ***Sensor Source Impedance***

- **Affects the amplifier's input bias current specification**
  - Does the amplifier's input circuitry load significantly change the sensor's output?
- **Typical high impedance sensors**
  - pH Electrode
  - Piezoelectric transducer
  - Ion chamber
- **Typical low impedance sensors**
  - Thermocouple
  - Resistive bridges
  - LVDT



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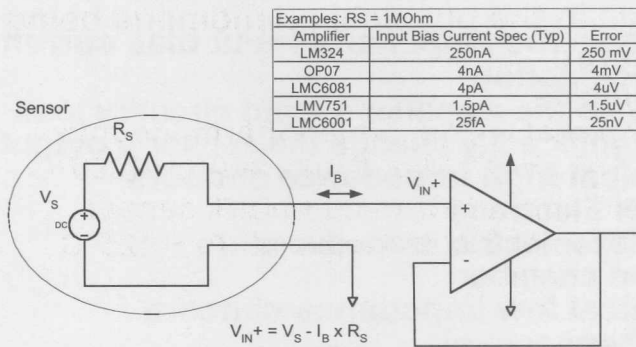


The input bias current of the amplifier will load the sensor's output. High source impedance sensors such as pH electrodes, piezoelectric transducers, and ion chambers will require amplifiers with pico-amp input bias currents. Low impedance sensors such as thermocouples and resistive bridges could use amplifiers with input bias currents in the nano-amp level.

The amplifier's input bias current also interacts with the feedback network to generate an additional error term in the amplifier's output.



## Input Bias Current Induced Errors



Error due to Amplifier's input bias current and the source resistance of the sensor.

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*CMOS  
changes  
bias current  
double for  
every 10°C*

Here is an example of the effect the input bias current has on the sensor's output. This sensor is a voltage-output sensor with a source impedance of one megohm. The table lists the typical input bias currents for five different amplifiers. The LM324 and OP07 are bipolar inputs while the LMC6081, LMC751 and LMC6001 are FET input amplifiers.

The bipolar input amplifiers have a large error relative to the FET input amplifiers. It is also useful to note that amplifiers, such as the LMC6001, are available with tested, sub pico-amp, input bias currents.

## **Sensitivity**

- The change in the sensors output for a change in the physical phenomena being measured

- Examples

- Chromel – Constantan thermocouple
  - $\sim 76 \mu\text{V}/^\circ\text{C}$  Max temperature  $\sim 1000^\circ\text{C}$
- Semiconductor temperature sensor
  - $10 \text{ mV}/^\circ\text{C}$  Max temperature  $\sim 125^\circ\text{C}$

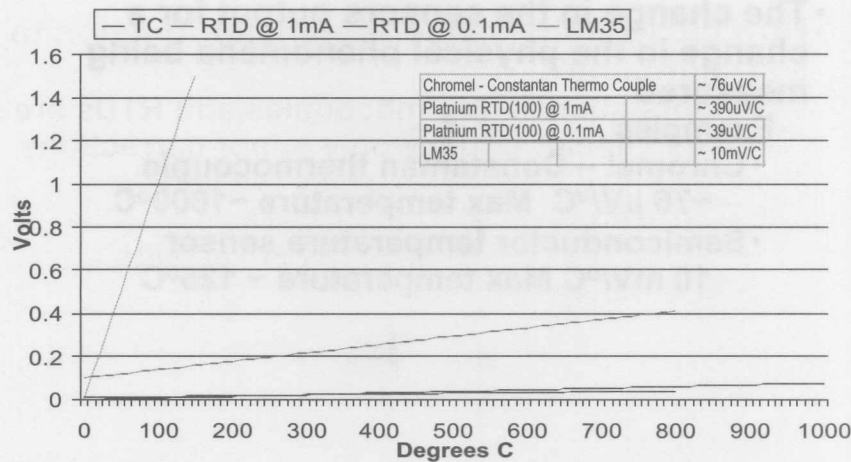


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The sensitivity of a sensor specifies how much the output of the sensor change for a unit change in the measured variable. Using a thermocouple and semiconductor temperature sensor as an example, a Chromel-Constantan thermocouple has a sensitivity of about  $76 \mu\text{V}/^\circ\text{C}$  while a semiconductor temperature sensor has a sensitivity of  $10 \text{ mV}/^\circ\text{C}$ .

## Temperature Sensor Sensitivity



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Here are several examples of sensor sensitivity. The graph and table shows an LM35, a semiconductor temperature sensor, a Chromel-Constantan thermocouple, and a RTD with two excitation current levels.

This shows how the sensitivity of an active sensor can be changed to meet specific requirements. A Platinum RTD (100) has 100 Ohms resistance at 0°C. With 0.1 mA excitation current, it has an output of about 39 mV/°C and at 1 mA excitation current, it has an output of about 390 mV/°C. The choice on which current to use could be based on other factors, such as minimizing the self-heating of the RTD.

## Linearity

- How close is the sensor's transfer function to a straight line?
  - Sensors such as thermocouples and RTDs are close to linear. Usually only minor corrections needed if additional accuracy needed
  - Sensors such as thermistors are very nonlinear and are usually linearized with lookup tables



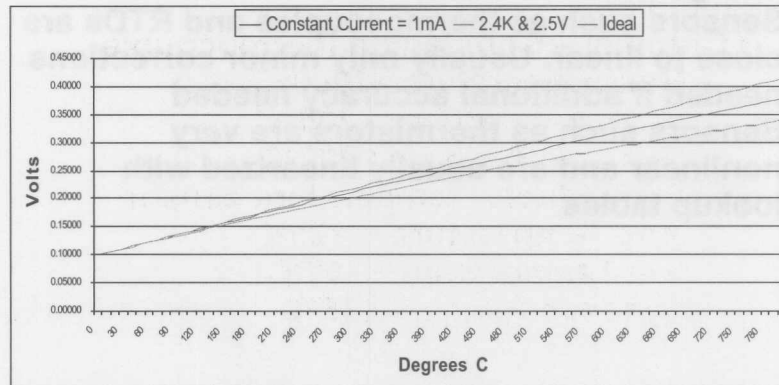
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Linearity specifies how close the sensor's transfer function is to a straight line. A linear transfer function is usually desirable because it simplifies converting the sensor's output to the actual value of the measured stimulus.

Some types of sensors such as RTDs, thermocouples, and bridges have close to linear transfer functions. Sensors such as thermistors have very nonlinear transfer functions and in many cases are linearized after the ADC conversion with lookup tables by the microcontroller.

## Driving Active Sensors



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How an active sensor is being excited can affect its linearity. This graph shows the effect of using constant current excitation vs a constant voltage excitation on a RTD.

The ideal curve is the slope of the RTD's transfer function extended to 800°C. The middle curve is the transfer curve of the RTD using 1 mA excitation current. This curve shows the small reduction in sensitivity of the RTD as the temperature increases.

The third curve shows the results of using a constant voltage source and a series resistor to excite the RTD. The series resistance is sized to provide a 1 mA current at 0°C when the RTD's resistance is 100 Ohms. The curve shows the second error term introduced by this type of excitation. As the resistance of the RTD increases, the RTD and the series resistor form a voltage divider that further decreases the linearity at higher temperatures.

## ***Dynamic Range***

- The minimum to the maximum value of the physical phenomena to be measured

- Examples

- Chromel – Constantan thermocouple

- Max temperature ~1000°C

- Min temperature ~ -200°C

- Dynamic Range = 1200°C

- Semiconductor temperature sensor

- Max Temperature ~ 125°C

- Min Temperature ~ -40°C

- Dynamic Range = 165°C



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The dynamic range of a sensor is the span of the stimulus for which a usable output is available. Two factors could limit the dynamic range. The first is saturation. Saturation is the rapid loss of sensitivity above or below a given level of the stimulus. A second limit to the dynamic range is material failure. Above a material limit level of the stimulus, the sensor will be damaged or destroyed. Thermocouple metals can melt if the temperature is too high, or a pressure transducer can rupture if the pressure being measured is too high.

## ***Frequency Response***

- The frequency response can vary over a wide range
  - Geophysical measurements will range from one cycle per day to several Hz
  - Factory processes may range from 0.001 Hz to several kHz
  - Radiation measurements may have pulses with nSec width requiring an amplifier with a GHz bandwidth



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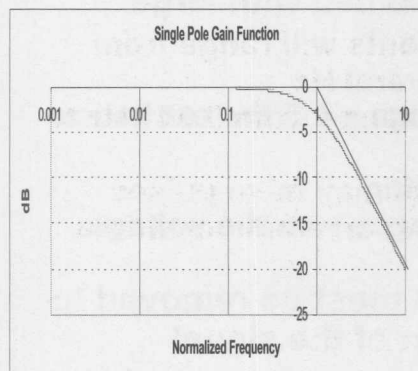


The signal frequencies of the sensor's output will depend on the type of measurement being made and can range from cycles per day for geophysical measurements to hundreds of megahertz for some types of radiation measurements.

The required closed-loop bandwidth of the amplifier will depend on the frequency components of the sensors output and the gain accuracy needed for those components.



## Closed-Loop Bandwidth



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System Resolution	Normalized Bandwidth for < 1/2 LSB Error
8 bit	0.062592
9 bit	0.044227
10 bit	0.031261
11 bit	0.022101
12 bit	0.015626
13 bit	0.011049
14 bit	0.007813
15 bit	0.005524
16 bit	0.003906

**What bandwidth is available?**

**Example:**

**LMP2011: GBW = 3 MHz**

**At a gain of 20 the BW =  
150 kHz**

**For 12-bit accuracy  
max signal frequency is  
 $0.0156 \times 150 \text{ kHz} = 2.34 \text{ kHz}$**

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This graph and table is a method for estimating the effective bandwidth of an amplifier given its gain bandwidth product, closed-loop gain, and resolution of the system.

The normalized bode plot represents the specification given in the amplifier's datasheet which is the gain bandwidth (GBW). Typically, the GBW is the frequency where the amplifier's output is down by 3 dB. The -3 dB point represents a 29.3% error ( $100\% - 70.7\%$ ). This can be interpreted as the signal bandwidth to obtain a specified precision is substantially less than the -3 dB frequency.

The table shows how much bandwidth is available for a given precision.

Using the LMP2011 with a 3 MHz GBW as an example: At a closed-loop gain of 20 and a 12-bit accuracy requirement, the effective bandwidth of the amplifier is only 2.34 kHz. If the accuracy is increased to 16 bits, the effective bandwidth is only 590 Hz.

## **Common-Mode Signal Components**

- **Several types of sensors have small differential signals combined with large common-mode voltages**
  - **Bridge sensors**
    - **Common-mode voltage ~ 0.5 the excitation voltage**
  - **High-side current sensing**
    - **Common-mode voltages ~ to the voltage source.**
- **Common-mode voltage must be removed to recover the data portion of the signal**



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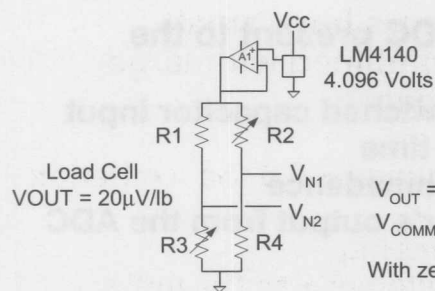


Bridge sensors will typically have the sensor's output signal riding on top of a common-mode voltage that is equal to about one half of the excitation voltage.

The current sensing resistor on a high-side current measurement circuit will have a common-mode voltage that is close to the supply voltage.

The common-mode voltage must be removed to recover the sensor's signal.

## CMRR Error Example



$$V_{OUT} = V_{N1} - V_{N2}$$

$$V_{COMMON MODE} = (V_{N1} + V_{N2}) / 2$$

With zero weight on the scale:  $R1=R2=R3=R4$

$$V_{COMMON MODE} = 4.096 / 2 = 2.048 \text{ Volts}$$

Amplifier's CMRR	CMRR Error	Weight Error
-100 dB	20.48 μV	1.02 lb
-80 dB	204.8 μV	10.2 lb
-60 dB	2048 μV	102 lb



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In this example, the effect of the amplifier's CMRR is shown with its contribution to the system error. This is a resistive bridge being used on a load cell to measure weight. The sensitivity of the load cell is 20 mV/lb and has a 4.096 V excitation voltage. The common-mode voltage at the bridge's output is 2.048 volts. The table shows the error with three values of CMRR. Even with 100 dB of CMRR there is an error of about 1 lb.

## ***Driving the ADC***

- **What load does the ADC present to the amplifier?**
  - **Most ADCs have a switched capacitor input**
    - **Amplifier's settling time**
    - **Amplifier's output impedance**
  - **Isolating the amplifier's output from the ADC input**

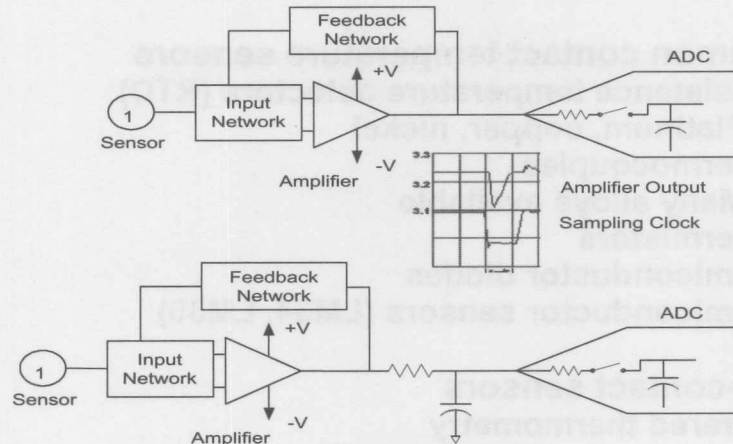


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The amplifier must be able to drive the ADC's input with a minimum of error. The challenge for the amplifier is that many ADCs have a switched capacitor on the input for sampling the amplifier's output. The amplifier must be designed for setting quickly with this type of load, or it will be necessary to find some way to isolate the ADC's input from the amplifier's output (see previous sections on amplifier stabilization).

## Amplifier-to-ADC Interface



Isolating the Amplifier from the ADC:  
R and C values Dependent on Amplifier, ADC and Signal Frequency

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The top schematic shows the ADC's input connected directly to the output of the amplifier. When the sampling capacitor in the ADC is connected to the amplifier's output, a charging current flows from the amplifier to the ADC, which causes a momentary glitch that can take some time to settle. One way to minimize this effect is to slow down the sampling rate. This provides the amplifier with the time necessary to stabilize its output.

A second way to minimize the error caused by the switch capacitor is to have a capacitor connected to the ADC's input. This capacitor is much larger than the internal sampling capacitor that provides the charge needed to quickly charge the ADC's sampling capacitor. An isolation resistor may also be needed to isolate the additional load capacitance from the amplifier's output.

## ***Temperature Sensors***

- **Common contact temperature sensors**
  - Resistance temperature detectors (RTD)
    - Platinum, copper, nickel
  - Thermocouples
    - Many alloys available
  - Thermistors
  - Semiconductor diodes
  - Semiconductor sensors (LM34, LM35)
- **Non-contact sensors**
  - Infrared thermometry



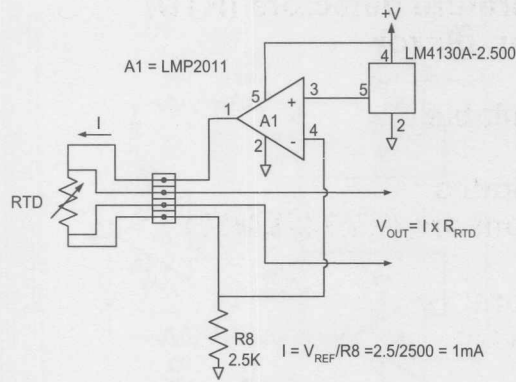
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Temperature is one of the most commonly measured properties and a variety of sensors have been developed for this purpose. Of these, the RTD and the thermocouple are widely used in industrial processes.

The next several slides show a RTD and a thermocouple amplifier circuit.

## Resistance Temperature Detector



- Current source design
- Low drift components
- RTD self-heating ( $I^2R$ ) thermal impedance
- For a temperature range of 0°C to 600°C, sensor resistance: 100Ω to 329.64 Ω
- V out: 0.1 to 0.32964 volts (Plus 2.5 volts CMV)
- Scale signal to 2.5 volts  
 $A_v = 2.5 / 0.32964 = 7.58$   
 (Includes the non-zero signal offset)

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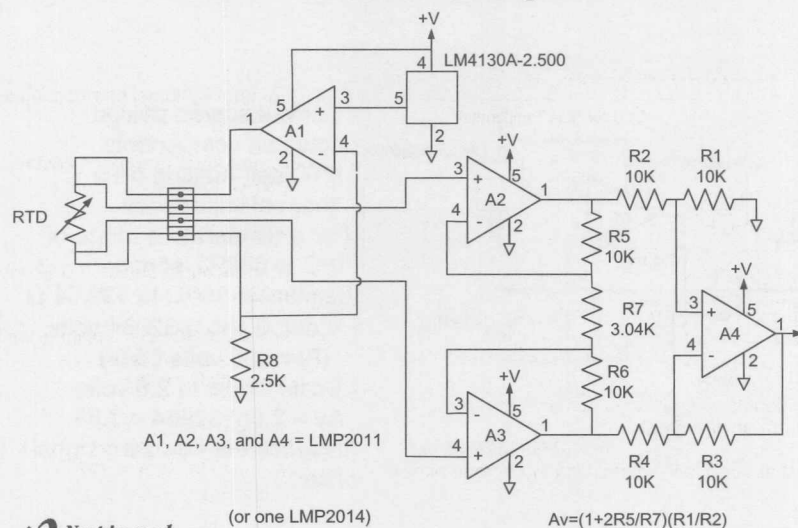
Here is the 1 mA constant current excitation for the RTD. The LM4130A-2.500 is the reference for the current source and the 2.5 K Ohm resistor is the current sense resistor. The combination of the LMP2011, the LM4130, and a precision 2.5 K Ohm resistor created an accurate and stable current source.

The RTD is shown with a 4 wire Kelvin connection. The current flows through the force leads, while the sense leads, which are precisely connected to the active resistor element, connect the voltage that is across the resistor to the signal amplifier.

Note that the RTD signal has three components to it. The temperature signal represented by change in resistance, an offset voltage due to the non-zero resistance at the starting temperature, and a common-mode signal of 2.5 volts due to the current sense resistor.



## RTD with Amplifier



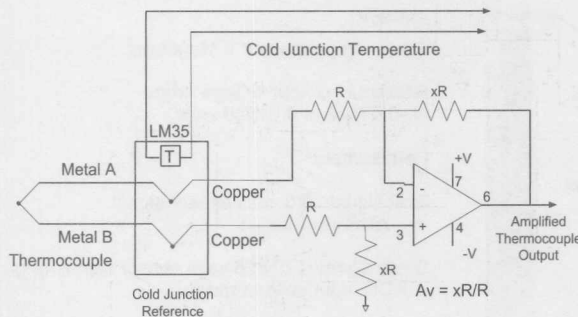
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The RTD signal is being scaled to 2.5 Volts full scale and the required gain is 7.58 (see the previous slide for the calculation). Three LMP2011 amplifiers are used to build an instrumentation amplifier or a single LMP2014 can provide this function including a buffer for the reference voltage. These amplifiers provide a high CMRR and low offset voltage and offset voltage drift.

## Thermocouple Interface



Thermocouple wire picks up common-mode noise from environment

Differential amplifier removes common-mode pickup

Chromel – Alumel thermocouple sensitivity =  $38.8 \mu\text{V}/^\circ\text{C}$

Temperature range to measure =  $50^\circ\text{C}$  to  $850^\circ\text{C}$

Cold junction  $\sim 25^\circ\text{C}$

Thermocouple output  $\sim 0.97 \text{ mV}$  to  $32.01 \text{ mV}$

Scale to ADC full scale input with  $V_{\text{REF}} = 2.048$  volts using a differential amplifier.

$A_v = 2.048/0.032 = 64$

For  $R = 2 \text{ k}\Omega$  Ideal  $xR = 128 \text{ k}\Omega$

Nearest 1% value =  $127 \text{ k}\Omega$

Actual gain  $\sim 63.5 \pm 1.3$

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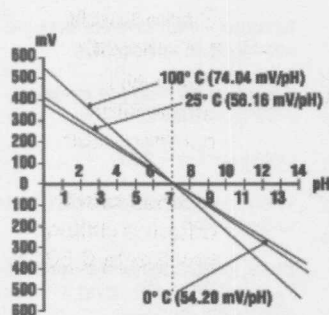
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Here is an example of a thermocouple amplifier. The thermocouple has a low source impedance so a single differential amplifier can be used. The differential input is used to remove common-mode noise that the wires pick up from the environment.

The thermocouple has a full-scale output of  $32 \text{ mV}$  in the temperature range of interest, and it is desired to scale this to  $2.048$  volts full scale. The required ideal gain is  $64$ .

Also shown is an LM35 being used to measure the cold junction reference temperature. The amplified thermocouple signal and the LM35 output go to an ADC for conversion.

## pH Electrode Interface



pH Electrode Transfer Function



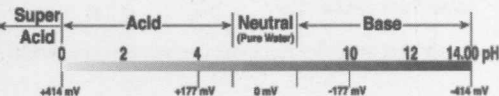
Source Impedance = 9 Megohms

Maximum output voltage range  
= -0.51828 to 0.51828 volts

Requirement

Shift signal: 0.0 volts sensor signal  
= \_ ADC input range

Scale signal: 1.03656 volts sensor signal range  
to ADC input voltage range.



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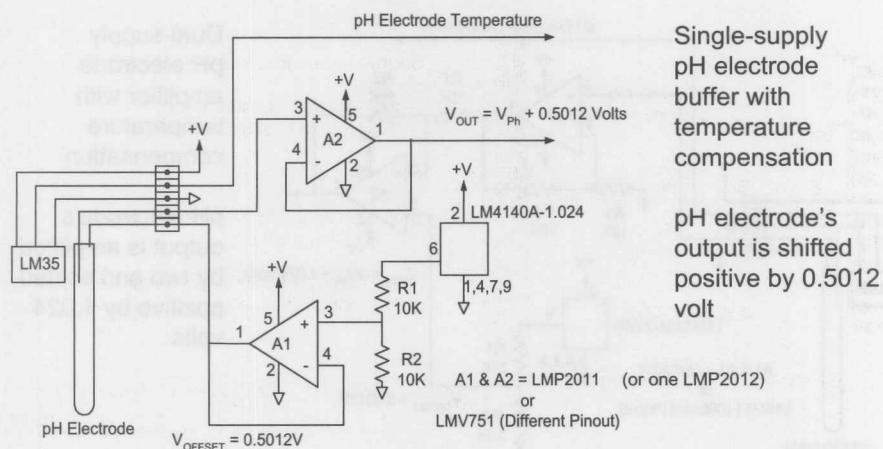
46

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The pH electrode is used to measure the pH of a solution. The graphs above show the physical relationship between the pH of a solution and the output voltage of the pH electrode, and its temperature dependence. The source impedance of the pH electrode is typically 106 Ohms to 107 Ohms. For most practical uses, the pH electrode must be buffered before driving the cable to the measurement instrument. Additionally to obtain an accurate measurement of pH the temperature of the pH electrode must be known.

Note that the output signal is bipolar and will require level shifting to be used in a single-supply system.

## pH Electrode Interface Ex1



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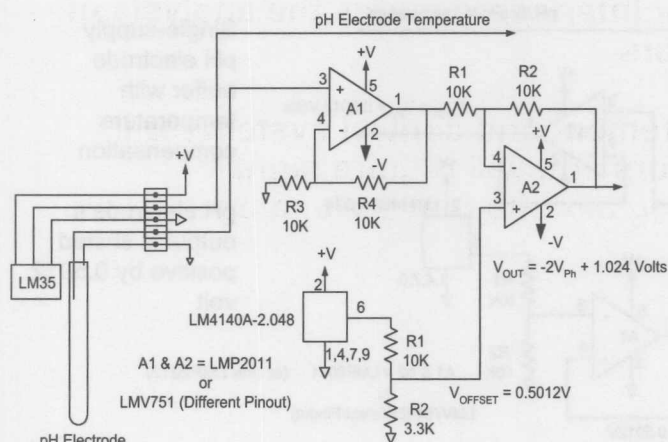
47

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The output voltage of a pH electrode is high enough to use without additional amplification. In this single-supply circuit, the pH electrode is offset by a little more the 0.5 volts by amplifier A1. The second amplifier A2 buffers the output of the pH electrode and drives the ADC. This circuit shifts the bipolar pH electrode signal to a unipolar signal for use in a single-supply system.

The LM35 is used to measure the temperature of the electrode so a temperature corrected pH measurement can be taken.

## pH Electrode Interface Ex2



Dual-supply  
pH electrode  
amplifier with  
temperature  
compensation

pH electrode's  
output is amplified  
by two and shifted  
positive by 1.024  
volts

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In this circuit, the pH electrode output is amplified and level shifted. The amplifier A1 has a gain of two in addition to providing a high input impedance buffer to the pH electrode. Amplifier A2 does the level shifting function so the signal is unipolar.

The LM35 is used to measure the electrode temperature.

## ***Summary***

- The sensor interface requires the analysis of many factors
- All measurement and control systems will have sensors and will require signal-conditioning circuits that are analog







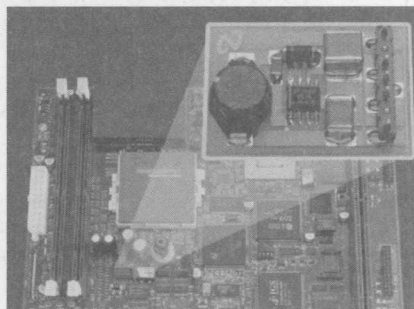


## **WEBENCH<sup>®</sup> Amplifiers Design Environment**

**[amplifiers.national.com](http://amplifiers.national.com)**

## **WEBENCH® Objective: Save System Designers Time**

- Get to working prototype quickly using National's WEBENCH online design and evaluation tools
- WEBENCH tools embed National's sub-circuit expertise, allowing designers to focus on areas of their expertise



2



The objective of the WEBENCH® online design environment has remained the same since its inception: save system designers time. Customers put their time and expertise into the development of a main board consisting of primarily digital components, and often do not want to spend a lot of time designing proprietary sub-circuits such as power supply circuits or Op-Amp gain stages. In addition, these analog sub-circuits may be outside their area of expertise.

However, each of the WEBENCH online tools embeds expertise of National's application engineers and device designers, incorporating best practices to improve the chances of success. They follow a step-by-step "wizard" approach, bringing the designer through the application specification, component selection, and appropriate simulations or evaluations. The goal is to quickly get to a working prototype in which the designer has high confidence.

## WEBENCH Online Design Tools

Amplifiers <small>NEW!</small>	<ul style="list-style-type: none"> <li>• Design Custom Filter or tailor preconfigured circuits to your requirements</li> <li>• Evaluate with online electrical simulation</li> </ul>
Audio <small>NEW!</small>	<ul style="list-style-type: none"> <li>• Select the best audio amplifier for your design</li> <li>• See thermal and frequency response</li> </ul>
Power	<ul style="list-style-type: none"> <li>• Design and optimize power supplies using online electrical and thermal simulations</li> <li>• Get a custom prototype kit fast</li> </ul>
Wireless	<ul style="list-style-type: none"> <li>• Optimize your PLL loop filter</li> <li>• Includes VCO selection, filter calculation and simulation</li> </ul>



3



At WEBENCH.NATIONAL.COM, National can provide the customer with applications that are customized to the specifications of the customer's design. A variety of online simulation and calculation tools aid in evaluating the performance of the applications.

Several types of systems are currently supported, now including tools for amplifiers and audio applications.

## **WEBENCH Amplifier Online Design Tools**

- Tailor and evaluate Op-Amp applications to meet your system requirements
- Simple process yields quick solutions
  1. Select application
    - Preconfigured applications
    - Active filter designer
  2. Enter system requirements
  3. Select Op-Amp from list
  4. Other circuit components selected automatically
  5. Evaluate application with online SPICE simulation



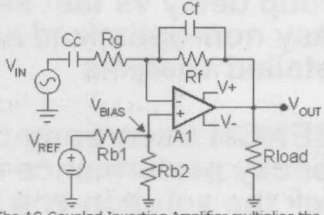
4



The WEBENCH amplifier online design tools provides a safe, structured environment in which many op amp applications may be tailored and then evaluated.

Two types of applications are available: Preconfigured topologies and topologies created using a wizard, such as the Active Filter Designer. In general, the process for designing either type of application is the same. The user enters system requirements which are then interpreted into component and topology requirements, and preferences. The user then selects from a list of suitable Op-Amps for that design. After the remaining circuit components are selected, the application may then be evaluated in the online SPICE simulation environment.

## Choose and Preview Application

Select Topology	Your Selection:
<b>Preconfigured Amplifier Circuits</b> <b>Popular Applications</b> <ul style="list-style-type: none"> <li><input type="radio"/> NonInverting Amp</li> <li><input type="radio"/> Inverting Amplifier</li> <li><input checked="" type="radio"/> AC-Coupled Inverting Amp</li> <li><input type="radio"/> AC-Coupled NonInverting Amp</li> </ul>	<b>AC-Coupled Inverting Amp</b> <span>→ NEXT</span>
<b>Instrumentation &amp; Signal Conditioning</b> <ul style="list-style-type: none"> <li><input type="radio"/> Integrator</li> </ul>	 <p>The AC-Coupled Inverting Amplifier multiplies the non-DC input voltage by the desired negative gain:  <math display="block">V_{out} = [-(R_f/R_g) \times V_{in(p-p)}] + V_{bias}</math></p> <p>Vbias is added to the op amp noninverting input to bring that input pin voltage within the normal operating range of the amplifier. It also provides an offset for the output, so that it is within its operating range.</p>
<b>Preconfigured Active Filters</b> <ul style="list-style-type: none"> <li><input type="radio"/> Lowpass Filter</li> <li><input type="radio"/> Highpass Filter</li> <li><input type="radio"/> Lowpass Filter 4th Order</li> </ul>	
<b>Active Filter Designer</b> <ul style="list-style-type: none"> <li><input type="radio"/> Custom Filter</li> </ul>	



Also see Op-Amp Product Folders!

5



All available topologies are shown on the WEBENCH for amplifiers home page. Selecting a topology on the left displays a summary of the topology on the right. The schematics display additional information that is displayed when the mouse is held over a component or portion of the circuit.

When the user has decided which topology to use, the "Next" button will move the user to the next page to enter the system requirements.

Op-Amps that are supported by WEBENCH Amplifiers topologies have a WEBENCH entry panel in their product folder. This allows the user to create an online design using a specific Op-Amp, rather than selecting from a list. If the Op-Amp is not capable of supporting the system requirements, error messages will guide the user to a successful solution.

## **WEBENCH Active Filter Designer**

- **Analog filter design is balance of tradeoffs**
  - Filter order vs component cost
  - Near-ideal frequency response vs constant group delay vs fast settling time
  - Easy non-optimized solution vs high-quality detailed analysis
- **WEBENCH uses easy design process**
  - Specify performance requirements
  - Pick the solution you like
  - Select Op-Amp from prescreened list
  - Evaluate filter online



6



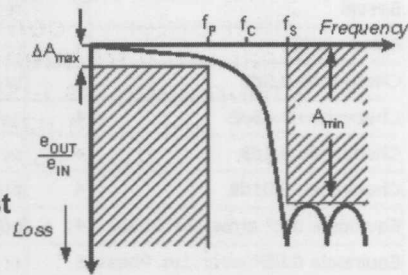
While the preconfigured topologies have fixed schematics, the Active Filter Designer adapts the schematic to the system requirements and the user's choice of trade-offs. An analog filter is an approximation of an ideal filter, and its design involves balancing many trade-offs. There is no one best solution!

A filter design is characterized by its response, order, and cutoff frequency. Many responses have been developed, such as Bessel, Butterworth, and Chebyshev, and each addresses performance trade-offs in different ways. In addition, the order of the filter (e.g. typically the number of poles in a low pass filter) sets the steepness of the frequency response, at the penalty of additional components needed to realize the circuit. Historically, a large amount of math has been needed to figure the component values needed for a multi-order filter. Online filter design tools have been limited in scope, making it difficult to clearly see the trade-offs and/or design options.

Using the WEBENCH Active Filter Designer allows the user to focus on system requirements, and let National's "back-end" computing horsepower take care of the math. Several solutions are presented in a manner that allows the user to see the performance trade-offs. After the Op-Amp is selected from a prescreened list, the rest of the design is created. And, as with the preconfigured topologies, the resulting circuit can be evaluated using online SPICE simulation.

## Option 1: Specify Performance

- Filter frequency response
  - Defined by profile
  - In passband ( $F < F_p$ )
    - Gain must be within  $\Delta A_{\max}$  of nominal gain
  - In stopband ( $F > F_s$ )
    - Attenuation must be at least  $A_{\min}$
  - In cutoff region ( $F_p < F < F_s$ )
    - $F_c$  used to define filter
    - $F_c$  may need adjustment
    - As  $(F_s - F_p)$  gets small, filter order gets big



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The filter design process may be started in one of two ways: specify the performance, or specify the filter response. We'll look at the specify the performance option first.

The frequency response is defined by a profile. The gain must be within  $\Delta A_{\max}$  of the nominal gain within the passband, and must be attenuated by at least  $A_{\min}$  in the stopband. The narrower the gap between the passband and stopband, the higher the filter order is likely to be (and the closer the filter response will be to ideal).

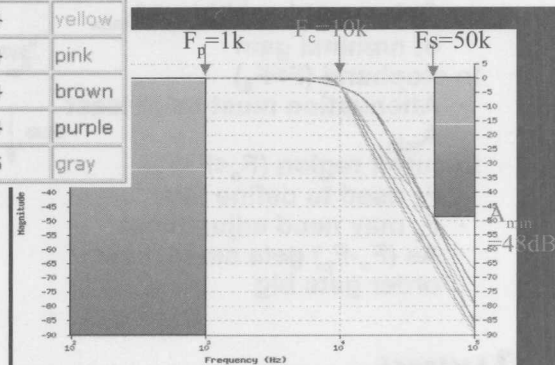
Cutoff frequency,  $F_c$ , is a value between  $F_p$  and  $F_s$ . It is used to calculate candidate responses as well as the required component values. It may be useful to vary  $F_c$  to see if lower orders can be used or if other measures of performance can be improved.



## See and Compare Candidates

Response	Order	Color
Bessel	5	red
Butterworth	4	cyan
Chebyshev 0.5dB	3	orange
Chebyshev 0.25dB	4	yellow
Chebyshev 0.1dB	4	pink
Chebyshev 0.01dB	4	brown
Equiripple 0.5° error, Lin. Phase	4	purple
Equiripple 0.05° error, Lin. Phase	5	gray

Each of these ideal filters meet the desired frequency response!



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Based on the user's frequency response requirements, more than 10 filter responses are evaluated. If the response can achieve the desired performance with an order of less than 10, it will be presented in the list of candidates.

The performance of all the candidates is shown in graphs, so the user can compare them.

The specific example used here is:

Passband:  $F_p = 1 \text{ kHz}$ ,  $DA_{\max} = 0.1 \text{ dB}$

Cutoff:  $F_c = 10 \text{ kHz}$

Stopband:  $F_s = 50 \text{ kHz}$ ,  $A_{\min} = 48 \text{ dB}$

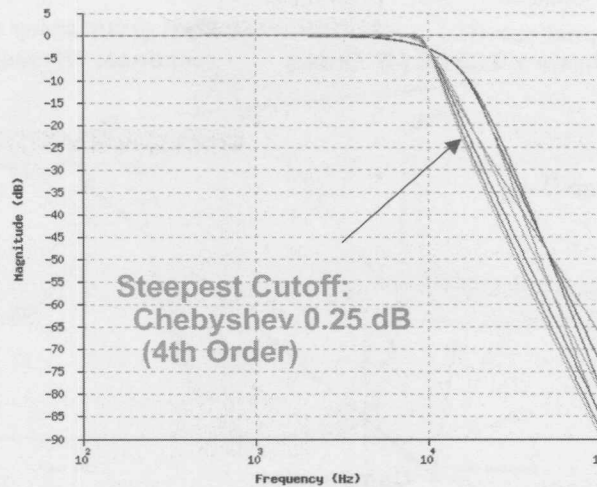
(The profile is overlaid on the resulting frequency responses for illustration.)

The list of filter candidates includes four versions of Chebyshev and two versions of Equiripple with Linear Phase. The Chebyshev response is defined by the amount of gain "ripple" allowed in the passband. While the gain ripple is not ideal, the Chebyshev tends to have the steepest rolloff of the standard filter types. Five variations of Chebyshev are evaluated, with gain ripple from 0.01 dB to 1 dB.

The Equiripple with Linear Phase response is defined by its phase error. Two popular variations are used here.



## Which Solution is Best?



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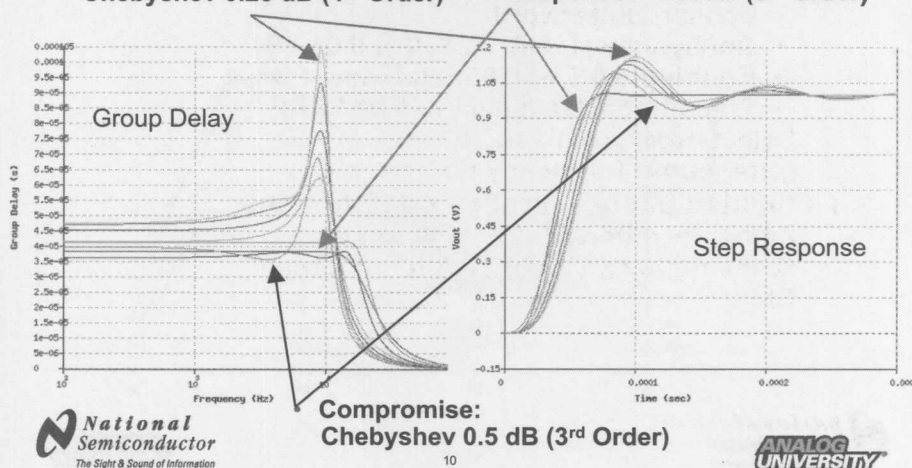
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The next step in the design process is to select the filter response that is “best.” If we consider only one measure of performance, frequency response, that’s not difficult. The response with the sharpest corner and the steepest roll-off is the Chebyshev 0.25 dB, 4<sup>th</sup> order.

It’s important to remember that, at this point, the graphs show ideal performance for each filter response. Later in the process, after the filter has been implemented with real components, a more realistic view of the performance can be seen.

## Best Frequency Response Isn't Always Best Solution

- Steepest cutoff: Chebyshev 0.25 dB (4<sup>th</sup> Order)
- Best group delay and step response: Bessel (5<sup>th</sup> Order)



The most ideal frequency response was produced by the Chebyshev 0.25 dB 4th order filter. However when we look at two other measures of performance, we see that it may not be the best choice for the system.

Group delay is a measure of how much the filter phase delay varies with signal frequency. Bessel and the Equiripple Linear Phase responses tend to have the least variation. A steady group delay contributes to a smooth step response.

All three graphs, plus phase response, are presented to the user so that appropriate trade-offs can be made.

This example will continue in a few slides using the Chebyshev 0.5 dB 3rd order transfer function, which offers a balance between sharp frequency response and fast settling time.

## **Option 2: Specify Response(s)**

- Choose up to four response/order pairs
  - Select from 11 responses
    - Bessel, Butterworth
    - Chebyshev (1, 0.5, 0.25, 0.1, 0.01 dB)
    - Equiripple 0.5 or 0.05deg/Linear Phase
    - Transitional Gaussian to 6 or 12 dB
  - Select order from 2 to 10
  - Enter cutoff frequency  $F_c$
- Facilitates user-controlled comparisons
  - Same  $F_c$ , different response/order
  - Same response and  $F_c$ , different order
  - Etc



The second option for starting the Active Filter Designer is to directly specify up to four responses to be evaluated and compared. Each response is described by a selection of the response type, the desired order, and the cutoff frequency. This approach is useful when the webench designer is used for educational purposes or to try out variations of a filter design.

After the filters have been defined, the same four graphs described previously are presented. When the user is ready, one filter response is selected for implementation.

## Optimization Tools

- **Adjust ideal frequency response for**
  - Group delay target
  - Step response/settling time target
- **Customize design for**
  - Gain
  - Supply voltages
  - Input signal levels
- **Optimize component selection for**
  - Low noise
  - Low power
  - High DC precision



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In addition to the basic filter design procedure illustrated in the preceding pages, there are several ways to optimize the design for even better performance. After candidate filters are identified that meet the frequency response requirements, the cutoff frequency of each filter is adjusted (if necessary) to meet targets for group delay or settling time. The "before" and "after" performance results are shown so that the better overall solution can be chosen.

Once the ideal filter response is selected, implementation begins. The user is requested to enter the desired system gain, supply voltages, and input signal amplitude and bias. In addition, one or several "environmental" options can be selected. If the application is to be low noise, then the gain per stage is adjusted so that the first stage dominates and limits the total noise. If the filter must operate with low power consumption, the Op-Amp selection has a preference for supply current less than 100  $\mu\text{A}$  per channel (vs 1 mA for a standard design). If the design needs high DC precision, then the Op-Amp selection has a preference for those with offset voltage less than 0.5 mV, bias current less than 100  $\mu\text{A}$ , and open-loop gain greater than 66 dB.

The system values entered by the user, combined with the frequency response requirements already set, are used to produce a list of Op-Amps which are appropriate for use in this filter implementation.

## After Choosing Ideal Response, Select Pre-Screened Op-Amp

Part Number	Pkg	Bandwidth at Closed Loop Gain of 2 (MHz)	Feedback Type (voltage or current)	Min. Closed Loop Gain (V/V)	Max. Supply Voltage (V)	Min. Supply Voltage (V)	VCM Min from Negative Supply (V)	VCM Max from Positive Supply (V)	Vout Max vs Positive Supply (V)	Vout Min vs Negative Supply (V)	Gain-Bandwidth Product, typ (MHz)	Supply Current typ per channel (mA)	Number of Channels	Inpt Offs Volta max 254 (mV)
<input type="radio"/> LMV342MM LMV342.MOD		0.5	VFB	1	5	2.7	-0.2	-0.8	-0.007	0.007	1	0.107	2	5
<input type="radio"/> LMV342MA LMV342.MOD		0.5	VFB	1	5	2.7	-0.2	-0.8	-0.007	0.007	1	0.107	2	5
<input type="radio"/> LMV344MT LMV342.MOD		0.5	VFB	1	5	2.7	-0.2	-0.8	-0.007	0.007	1	0.107	4	5
<input type="radio"/> LMV344MA LMV342.MOD		0.5	VFB	1	5	2.7	-0.2	-0.8	-0.007	0.007	1	0.107	4	5
<input type="radio"/> LMV341MG LMV342.MOD		0.5	VFB	1	5	2.7	-0.2	-0.8	-0.007	0.007	1	0.107	1	4
<input checked="" type="radio"/> LMV772MM LMV771.MOD		1.75	VFB	1	5	2.7	0	-0.9	-0.06	0.06	3.5	0.6	2	1
<input type="radio"/> LMV774MT LMV771.MOD		1.75	VFB	1	5	2.7	0	-0.9	-0.06	0.06	3.5	0.6	4	1
<input type="radio"/> LMV932MA LMV921.CIR		0.75	VFB	1	5.5	1.8	-0.2	0.2	-0.035	0.035	1.5	0.116	2	5.5
<input type="radio"/> LMP2011MF LMP2011.MOD		1.5	VFB	1	5	2.7	-0.3	-1.8	-0.081	0.091	3	0.93	1	0.05

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Each of the Op-Amps in the table of recommended parts is required to meet the requested supply voltage(s), and must be able to support the bandwidth and gain expected of each filter section.

Other characteristics are treated as preferences, i.e. it would be nice to have an output swing that's sufficient for the desired output voltage, but it's not required. Any parametric value that doesn't meet the preferred value is highlighted.

The example used to produce this list of Op-Amps was this:

- Gain = 10
- $V_{inAC} = 0.1$  V,  $V_{inDC} = 0$  V
- Supply =  $\pm 2.5$  V
- No special optimizations

Under each part number, the SPICE model name is given. Several parts may use the same model, differing only in the number of op amps per package. The model can be downloaded for use in an offline SPICE simulator.

The same Op-Amp part number is used in all instances in the filter design.

## Topology Wizard

- Select topology for 1<sup>st</sup> and 2<sup>nd</sup> order sections
- See parts list for each section
- Preview schematic
- When ready, go to “Analyze”

### Chebyshev 0.5dB Filter Order 3

#### Select First Order Section

- ☐ Section A  
☒ Section B

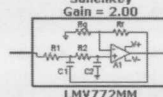
#### Section A

##### Select Topology

- ☒ SallenKey  
☐ MultipleFeedback

#### SallenKey

Gain = 2.00



LMV772MM

Components
C1 0.056 uF
C2 0.056 uF
R1 536 Ohm
R2 180 Ohm
Rf 1 kOhm
Rg 1 kOhm

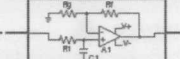
#### Section B

##### Select Topology

- ☒ FirstOrder\_PassNonInvert  
☐ FirstOrder\_ActiveInvert

#### FirstOrder\_PassNonInvert

Gain = 5.02



LMV772MM

Components
C1 0.027 uF
R1 1.1 kOhm
Rf 1 kOhm
Rg 249 Ohm



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With the Op-Amp selected, the rest of the solution can be developed. The Topology Wizard shows how many filter sections will be needed to realize the filter and allows the user to select the topology and placement of each section. The order of all sections is added up to match the desired total. In this case, we are designing a Chebyshev 0.5 dB 3rd order filter. Both 2nd and 1st order topologies are available, so the Wizard has selected one 2nd order and one 1st order section. The 1st order section is by default at the output end of the filter, but it can be moved to the front if desired.

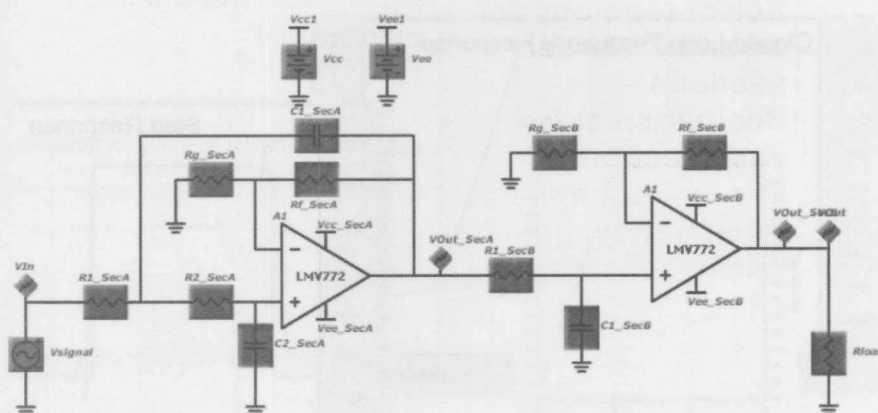
2nd order section topologies include Sallen-Key (SK) and Multiple Feedback (MFB). Sallen-Key uses one more resistor than MFB. Sallen-Key offers positive gain, and MFB offers negative.

1st order section topologies include an Active Inverting design and a Passive Noninverting.

Gain is distributed through the sections. In a normal situation, a gain of 2 is used for as many 2nd order sections as possible, since it allows the two capacitor values to be identical.

Below the mini-schematics for each section is the component list for that section. Actual component values are shown, as this list results from a search through a real component catalog.

## Online Simulation Uses the Entire Multi-Section Implementation



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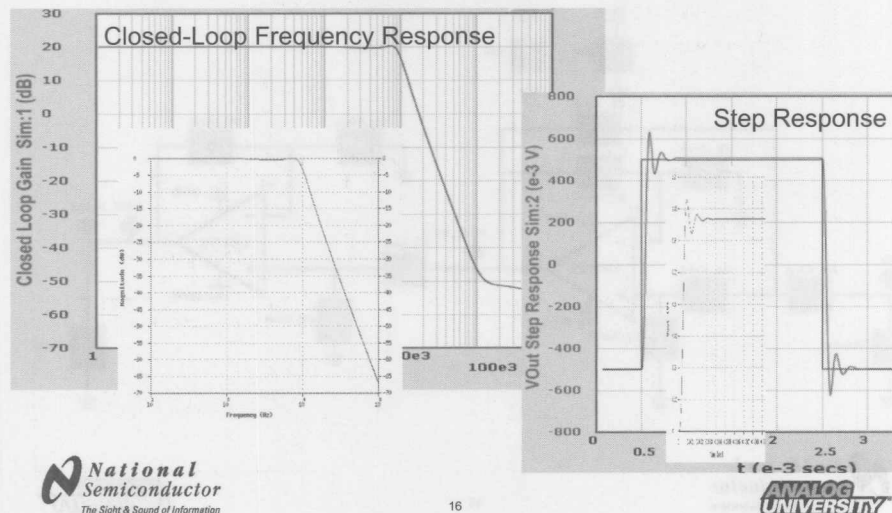


After the filter design has been configured in the Topology Wizard, it can be simulated. The design is translated into a net-list and schematic “on the fly”, and is imported into the online SPICE simulation environment.

Here, several tests can be run. Closed-loop frequency response and step response tests show the filter performance similar to the way it was presented during the earlier response selection step. Sine wave response allows the user to see if the output voltage of any of the sections is being limited, which degrades the performance of the circuit.



## Simulated Results Close to Ideal Responses

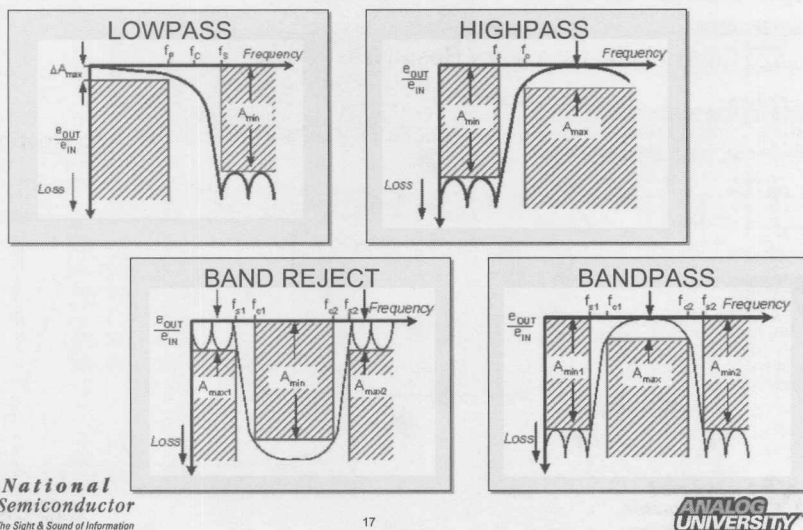


The Frequency and Step Response plots of this filter design match closely to the plots shown for the ideal Chebyshev 0.5 dB 3<sup>rd</sup> order filter. The two sets of plots are superimposed for comparison and scaled to match.

The primary difference in the simulated and ideal Frequency Response plots is the gain at higher frequencies. The ideal plot is purely mathematical, while the simulated plot takes into account the bandwidth limitations of the op amp used in the design as well as the non-ideal component values.

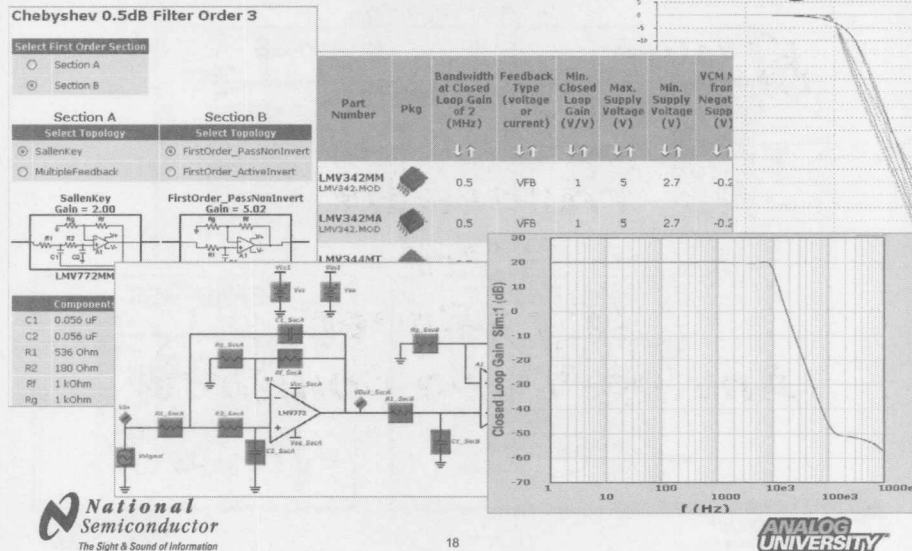


## Long-Term Capability: All Filter Types



During 2005, the WEBENCH Active Filter Designer will be expanded to include four standard filter types. Following the lowpass type which was the first to be available, highpass, band reject, and bandpass filter design support is being added.

# Design Your Filter in Minutes with WEBENCH Active Filter Designer



From specification of system requirements to topology development to component selection, WEBENCH Active Filter Designer can help you quickly develop a filter that meets your needs. Quickly select a filter response from several candidates without having to research through textbooks and do extensive calculations. Quickly develop a filter circuit that is ready to simulate online without having to assemble the SPICE schematic piece-by-piece. Try alternative solutions easily and share the best ones with colleagues. It really is that easy!



# **Appendix LMH<sup>®</sup> High-Speed Analog Video Solutions**

## **LMH<sup>®</sup> Amps and Buffers Singles:**

*High Performance:*                      Feature      LSBW MHz\*

LMH6702	OpAmp	Low Distortion	720
LMH6703	OpAmp	Shutdown	800
LMH6704	PGB	Av=+1,+2,-1	400
LMH6732	OpAmp	Variable Performance	540
LMH6559	Buffer	Av = +1	1000

*Value:*                                      Feature      LSBW MHz\*

LMH6714	OpAmp	Best DG/DP	250
LMH6720	OpAmp	Shutdown	250
LMH6723	OpAmp	1 mA Bias	180

\* Bandwidths are for Av = +2, Vout = 2 Vpp, RL = 100.

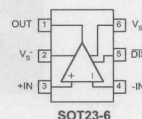
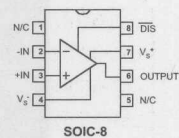


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## LMH6703: Single 1 GHz Op-Amp with Shutdown

- LSBW: 800 MHz ( $G = +2$  V/V, 2.0 V(p-p))
- Slew Rate: 3000 V/us
- Iout: 90 mA per channel
- Differential Gain/Phase: 0.02%/0.02°
- Very Low Distortion:  
- 2<sup>nd</sup> / 3<sup>rd</sup> : - 62/-78 @ 10 MHz
- Low Input Noise Voltage: 2.3 nV/ $\sqrt{\text{Hz}}$
- Shutdown
- Higher performance replacement for OPA695, AD8009, OPA691

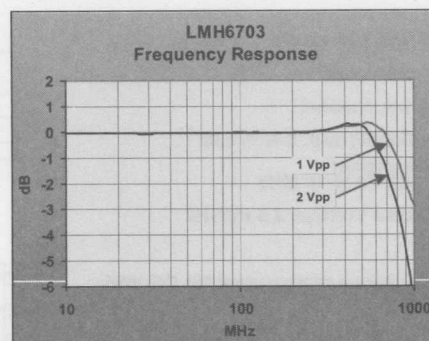


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## LMH6703: 1 GHz at 1 V(p-p)



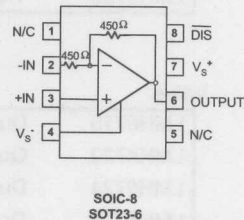
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## LMH6704: Single Programmable Gain Buffer

- Programmable Gain: -1, +1, +2 V/V
- SSBW: 800 MHz ( $G = +1$  V/V, 0.5 V(p-p))
- LSBW: 450 MHz ( $G = +2$  V/V, 2.0 V(p-p))
- Slew Rate: 3300 V/us
- Iout: 100 mA per Channel
- Differential Gain/Phase: 0.02%/0.01°
- Very Low Distortion:  
- 2<sup>nd</sup> / 3<sup>rd</sup> : - 80/-85 @ 5 MHz ( $V_o = 2$  V(p-p))
- Low input noise voltage: 1.8 nV/√Hz
- Disable
- Pin compatible with OPA682/692
- Replacement for HFA1112



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## LMH Amps and Buffers Duals, Triple and Quads:



High Performance:

Feature LSBW MHz\*

LMH6738	Triple Op-Amp	Shutdown	400
LMH6739	Triple PGB	Shutdown	400

Value:

Feature LSBW MHz\*

LMH6715	Dual Op-Amp	Best DG/DP	250
LMH6722	Quad Op-Amp		250
LMH6724	Dual Op-Amp	1 mA Bias	180
LMH6725	Quad Op-Amp	1 mA Bias	180



\* Bandwidths are for  $A_v = +2$ ,  $V_{out} = 2\text{ V(p-p)}$ ,  $R_L = 100\ \Omega$ .

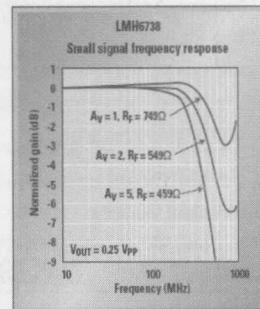
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## **LMH6738: 750 MHz Triple Video Op-Amp**

- SSBW: 750 MHz ( $G = +1$  V/V, 0.5 V(p-p))
- LSBW: 400 MHz ( $G = +2$  V/V, 2.0 V(p-p))
- Slew Rate: 3300 V/ $\mu$ s
- Iout: 90 mA per Channel
- Differential Gain/Phase: 0.02%/0.01°
- Very Low Distortion:  
- 2<sup>nd</sup> / 3<sup>rd</sup> : - 80/-90 @ 5 MHz ( $V_O = 2$  V(p-p))
- Low Input Noise Voltage: 2.3 nV/ $\sqrt{\text{Hz}}$
- Individual Disable
- Pin Compatible with OPA3691
- Higher Performance replacement for LT1399 and EL5364
- World's Fastest Triple Op-Amp



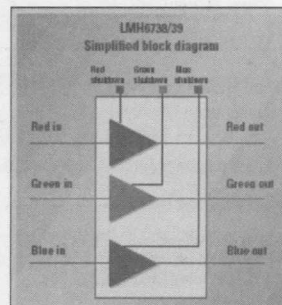
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## **LMH6739: 750 MHz Triple PGB**

- Programmable Gain: -1, +1, +2 V/V
- SSBW: 750 MHz ( $G = +1$  V/V, 0.5 V(p-p))
- LSBW: 400 MHz ( $G = +2$  V/V 2.0 V(p-p))
- Slew Rate: 3300 V/ $\mu$ s
- Iout: 90 mA per channel
- Differential Gain/Phase: 0.02%/0.01°
- Very Low Distortion:  
- 2<sup>nd</sup> / 3<sup>rd</sup> : - 80/-90 @ 5 MHz ( $V_o = 2$  Vpp)
- Low input noise voltage: 2.3 nV/ $\sqrt{\text{Hz}}$
- Individual Disable
- Pin compatible with OPA3692
- Higher performance replacement for  
LT6553/4, AD8074/5, EL5308
- World's fastest triple PGB



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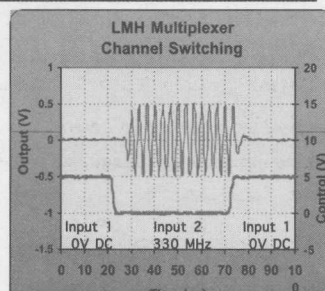
## LMH Analog Multiplexers



Configuration LSBW MHz\* Status

LMH6572	Triple 2:1	300	Available Now
LMH6574	4:1	400	Available Now
LMH6570	2:1	450	Available Now

Slew rate	2500 V/us
Channel switching	<10 ns
Switching glitch	<50 mV(p-p)
Gain flatness (0.1 dB)	200 MHz
Crosstalk (10 MHz)	-80 dB
Disable Mode =>	Hi Z Output



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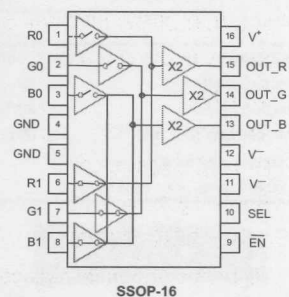
\* Bandwidths are for  $A_v = +2$ ,  $V_{out} = 2 \text{ V(p-p)}$ ,  $R_L = 100 \Omega$ .

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## LMH6572: Triple 2:1 Video Multiplexer

- Fixed gain of +2
- 400 MHz 200 mV  $-3$  dB Bandwidth
- 320 MHz 2V (p-p)  $-3$  dB Bandwidth
- Slew rate: 2200 V/ $\mu$ s
- Switching time (2V Step): 10 nS
- Differential Gain/Phase: 0.02%/0.04°
- Very low distortion:
  - 80 dB THD @ 5 MHz ( $R_L = 100\Omega$ )
  - 80 dB THD @ 5 MHz ( $R_L = 100\Omega$ )
- Low Crosstalk: -90 dB@ 5 MHz
- Pin-compatible replacement for LT1675



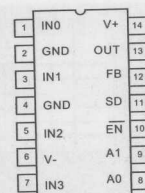
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## LMH6574: Single 4:1 MUX

- 700 MHz SSBW
- 450 MHz LSBW (@ 2 V(p-p))
- Slew rate: 2500 V/ $\mu$ s
- Shutdown
- Crosstalk: -80 dB
- DG/DP: 0.02%/0.02°
- Switching Time: 7 nS
- 14-Pin SOIC, TSSOP
- Higher performance replacement to the AD8174



SOIC

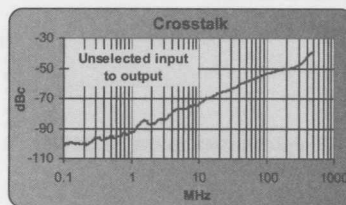
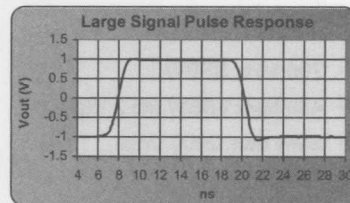
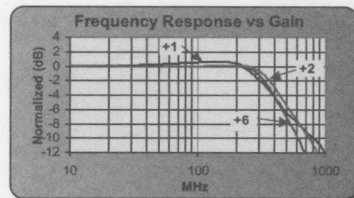
A1	A0	SD	EN	OUT
0	0	0	0	IN 0
0	1	0	0	IN 1
1	0	0	0	IN 2
1	1	0	0	IN 3
X	X	0	1	Hi Z
X	X	1	X	Hi Z



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## LMH6574 4:1 Mux



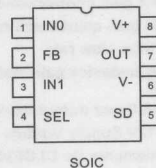
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## ***LMH6570: Single 2:1 MUX***

- 500 MHz SSBW (@ 500 mV(p-p))
- 400 MHz LSBW (@ 2 V(-p))
- Slew Rate: 2200 V/ $\mu$ s
- Shutdown
- All Hostile Crosstalk: -85 dB @ 5 MHz
- DG/DP: 0.02%/0.05°
- Switching time: 8 nS
- 8-Pin SOIC
- Higher Performance replacement for AD8170, MAX4158, LT1203, MAX4310, and MAX4313



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## **LMH6502 / LMH6503 / LMH6504**

### **Variable Gain Amplifiers**

#### **LMH6502/6503 variable gain amplifier**

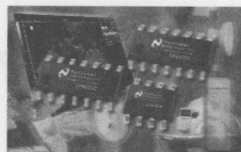
- 130MHz Signal Bandwidth
- 100MHz gain control bandwidth
- >70 dB gain adjustment range
- 1,800 V/ $\mu$ s slew rate
- Device-to-device gain matching within  $\pm 0.7$ dB
- $\pm 75$  mA linear output current
- 5V to 12V Supply Voltage
- Replacements for CLC520/522
- Available in TSSOP-14 & SOIC-14 Packages

Ideal for automatic gain control applications in test, measurement, and instrumentation equipment, video communications, and medical imaging



#### **LMH6504 variable gain amplifier**

- 150 MHz Signal Bandwidth
- 150 MHz gain control bandwidth
- 1,500 V/ $\mu$ s slew rate
- Device-to-device gain matching within  $\pm 0.42$ dB
- 11mA supply current
- Gain control is linear in dB
- Replacement for CLC5523
- Available in MSOP-8 & SOIC-8 Packages



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# **Audio Amplifier Applications**



## Audio WEBENCH® Tools: Enter Your Requirements



Audio Amplifier Selection - Basic Requirements			
Supply Type	Single Supply (+Vs) ▼		
Supply voltage (minimum)	2.7	V	<a href="#">help</a>
Supply voltage (maximum)	5.5	V	<a href="#">help</a>
Supply voltage (nominal)	5	V	<a href="#">help</a>
Load Impedance	8ohm ▼		<a href="#">help</a>
Output Power	1	W	<a href="#">help</a>
... at Total Harmonic Distortion (THD)	<input checked="" type="radio"/> 1% <input type="radio"/> 10%		<a href="#">help</a>

[Display Additional Selection Options](#)

[→ RECOMMENDED PARTS](#)



2

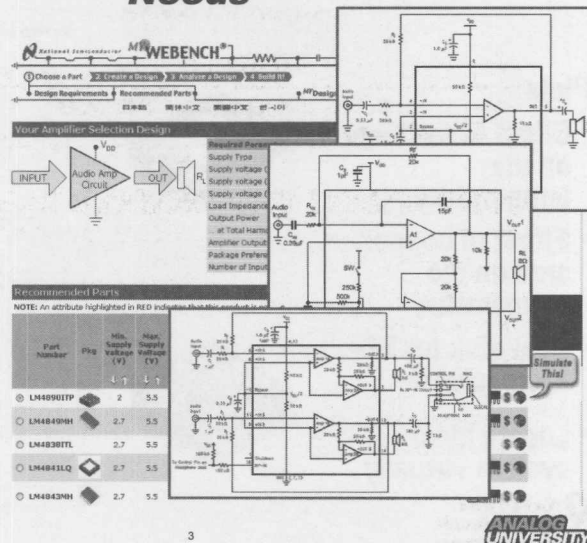


Audio WEBENCH® tools have recently been added to the WEBENCH tool suite. To begin the audio design process, enter audio amp parameters including supply voltage, load impedance and output power. Also, you can enter more advanced selection options

## Audio WEBENCH Tools: Find A Range Of Recommended Devices That Meet Your Needs

Evaluating  
several  
options is  
fast and easy

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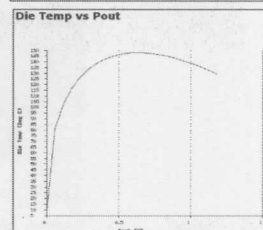
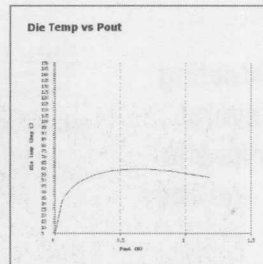
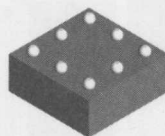
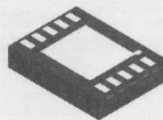


The WEBENCH tools will recommend a list of parts based on your inputs. You can choose the part that best meets your needs by comparing the features and parameters.

## Audio WEBENCH Tools: Thermal Behavior Trade-Offs Are Immediately Obvious

### Plots:

- Effect of package on die temperature
- Effect of copper area on die temperature
- Heat sink for TO-220 package
- Locate ideal system virtually



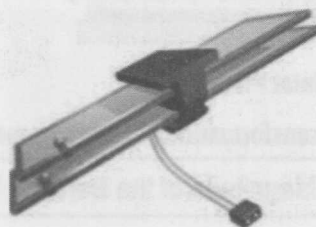
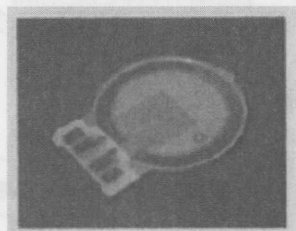
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You can see the effect of using different packages such as the LLP® or micro SMD package types. Also try different copper area and heat sinks.

## Ceramic Speakers and DMAs



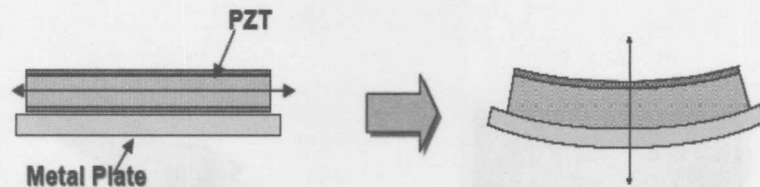
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The most common load for an audio amplifier is the moving coil speaker. The performance characteristics are usually measured assuming a resistive load in the range of 2 Ohms to 32 Ohms. Speakers that present a reactive load to the amplifier have been around for some time, but are now becoming increasingly popular in this age of miniaturization. This slide presents two new types of speaker technologies. On the left side, a ceramic speaker manufactured by Taiyo Yuden is presented, and on the right side a DMA (Distributed Mode Actuator) is presented. Both speakers use piezoelectric material in their design. We'll start with a discussion on ceramic speakers and later describe more about DMAs.

## Basic Concept of Piezo Speakers



Transformation of Piezo Element Movements into Bending Force

Magnitude of the Bending Vibration → Sound Pressure Level



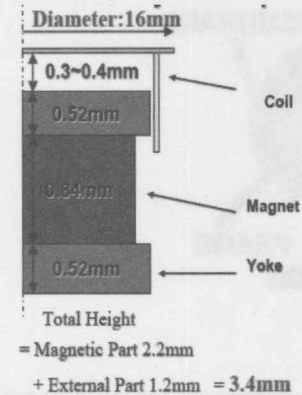
Elements that Reduce Bending Vibration

Hardness of the Metal, Mechanical Resistance, Air Resistance

Applying voltage across the terminals of piezoelectric material causes the material to expand or contract. When this material is mounted to a metal plate, the voltage differential translates into a bending force. The magnitude of this force translates into a sound pressure level (SPL).

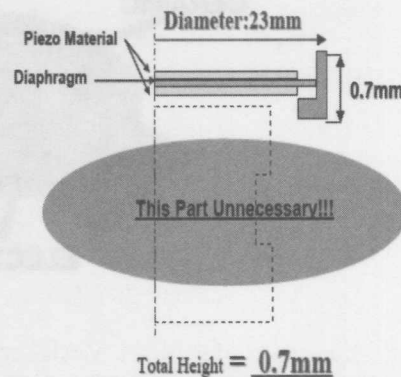
## Piezo Speaker

### DYNAMIC SPEAKER



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### CERAMIC SPEAKER

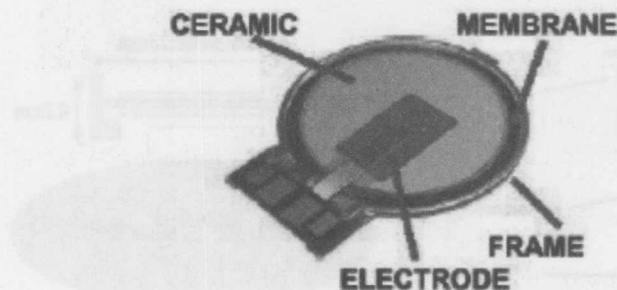


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A product designed with a dynamic moving coil speaker requires a much larger profile. A standard moving coil speaker consists of a coil, a magnet, and a yoke. It also requires approximately 1.2 mm of backspacing.

Ceramic speakers consist of a metal diaphragm, layers of piezo material, and a stub that holds both components together. The overall thickness of the speaker itself is 0.7 mm, which allows for thinner, more portable designs.

## ***Piezo Speaker Construction***



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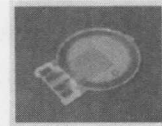
A piezoelectric ceramic loudspeaker is generally made of stacked layers of piezoelectric material, bonded to a metal plate. This is just one possible configuration. Also, there could also be stacked piezoelectric material bonded to both sides of the metal plate.

An example of a piezoelectric ceramic loudspeaker is shown above. Unlike moving coil dynamic speakers, piezoelectric ceramic speakers do not require a magnet or coil. An immediate advantage is that the speaker does not generate any magnetic fields that could interfere with other circuits in a tightly packed product.



## ***Electrical Characteristics of Ceramic Speakers***

- Frequency range – 100 Hz to 10 kHz
- Small and lightweight solution
  - Weighs less than 0.63 grams
  - Thickness is 0.7 mm
  - Diameter is less than 25 mm
- Capacitive load ( $\sim 2\mu\text{F}$ ) as opposed to resistive
  - Load impedance varies over frequency (low impedance @ high freq)
- Load voltage needed:  $\sim 15\text{Vp-p}$  for acceptable sound pressure level
  - Therefore, amplifier supply voltage = 7.5V
  - A *DC-DC converter is needed* to supply 7.5V to the audio amplifier using an available 3V-5V supply



**KEY ADVANTAGE:** More efficient than using moving coil speakers, even with DC-DC converter

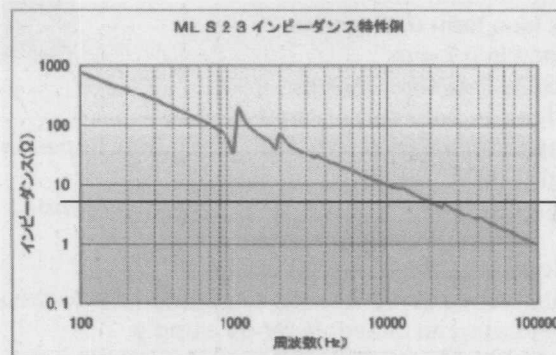
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## Load Impedance of Ceramic Speakers

Ceramic speaker has impedance characteristics similar to a capacitor



Load Impedance vs Frequency

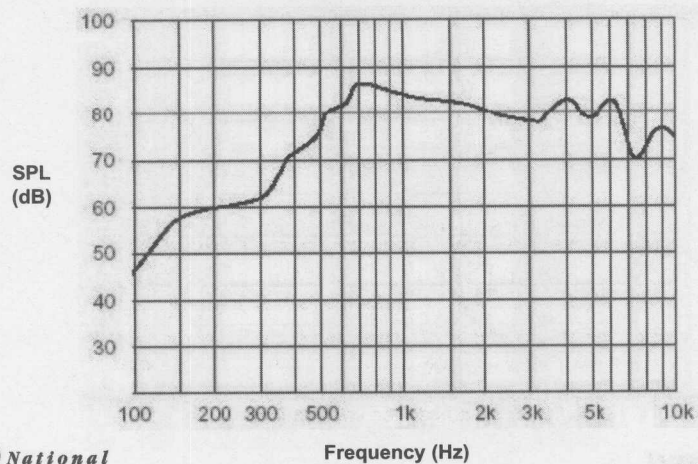
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Piezoelectric materials have high dielectric constants and their component electrical property is like a capacitor. Therefore, piezoelectric ceramic speakers represent essentially capacitive loads over frequency. A representative impedance vs frequency curve of a multi-layer piezoelectric ceramic speaker is shown above.

## Dynamic Speaker Frequency Response Comparison



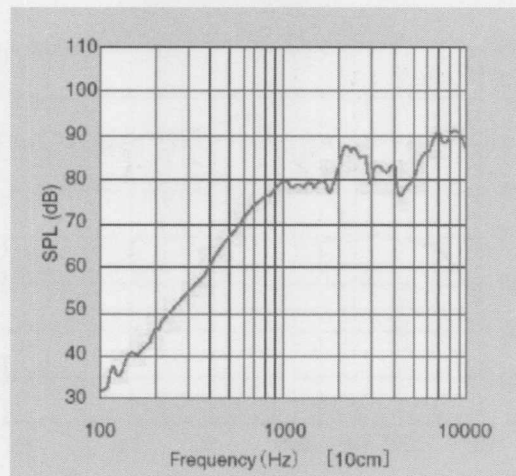
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The graph above shows SPL vs frequency for a typical miniature 20 mm diameter moving coil speaker.

## **Ceramic Speaker Frequency Response (Taiyo Yuden)**



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A representative SPL vs frequency curve of a 20 mm diameter multi-layer piezoelectric ceramic speaker is shown above, courtesy of Taiyo Yuden. The down side of using a ceramic speaker is the poor SPL at lower frequency levels.

## **Dynamic Speaker Power Dissipation**

**Simplified Equation:**

$$P_d = V^2 / R$$



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For most power calculations with a moving coil speaker, the assumption is that the power dissipation depends upon the resistance value of the coil and the driving voltage. If  $V = 2V$  and  $R = 16$  Ohms, then  $P_d$  would be 0.25 Watts. In the real world, the load has a reactive component over parts of the frequency ranges (by as much as  $60^\circ$ ), so the actual calculation of power dissipation is not straightforward. Since the spectral content of the source material is also not constant over the audio frequency range, assuming constant power vs frequency is conservative.

## ***Ceramic Speaker Power Dissipation***

**Equation:**

$$\begin{aligned} P_{\text{DIS}} &= ((CV^2)(2\pi f)(\cos\Phi) / 2) + ((CV^2)(2\pi f)(D_F) / 2) \\ &= (CV^2)(\pi f)(\cos\Phi + D_F) \end{aligned}$$

$$D_F = \tan\sigma$$

$\Phi$  is the phase angle between current consumption and voltage of a capacitor

$D_F$  is the dissipation factor of the ceramic material (varies from 0.017 to 0.123)

$\sigma$  is the dielectric loss angle (varies from 1° to 7° for ceramic speakers)



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For a piezoelectric capacitive load (not in resonance), the power dissipation equation is shown above. The first part of the equation is the capacitive power, and the second part of the equation is the power losses in the ceramic material itself.

The angle,  $\Phi$ , is the phase angle between the current consumption and the voltage. For a capacitor, this angle is 90° before in phase, and therefore  $\cos\Phi = \cos 90^\circ = 0$ .

This means that, ideally, the capacitive power consumption is zero, and the only losses are due to the dissipation factor (DF) of the ceramic material used and the frequency of operation. The higher the frequency, the higher the loss.

## ***Ceramic Speaker Power Dissipation***

Equation:

$$P_{DIS} = (CV^2)(\pi f)(D_F)$$

$D_F$  is the dissipation factor of the ceramic material (varies from 0.017 to 0.123)

$D_F = \tan\sigma$

$\sigma$  is the dielectric loss angle (varies from 1° to 7° for ceramic speakers)

**$P_{DIS}$  increases with frequency**



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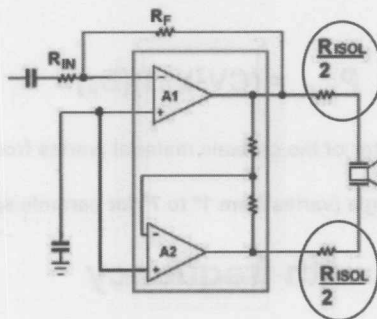
The dissipation factor (DF) for ceramic materials used for speaker purposes will vary depending upon the actual material used and the temperature of the material.

In a perfect dielectric, the voltage wave and the current are exactly 90° out of phase. As the dielectric becomes less than 100% efficient, the current wave begins to lag the voltage in direct proportion.

The amount of the current wave deviates from being 90° out of phase with the voltage is defined as the dielectric loss angle, or  $\sigma$ . The tangent of this angle ( $\tan\sigma$ ) is known as the loss tangent or the DF.

Loss angles in electro ceramic materials can vary from less than 1° to 3° for small signal conditions to as much as 7° for very high signal conditions.

## Amplifier Stability (BTL)



$R_{ISOL}$  prevents the amplifier from starting up into a load that looks like a short circuit

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Piezoelectric ceramic loudspeakers can be driven with standard audio amplifiers provided that adequate output voltages are available and the amplifier can drive the highly capacitive loads.

Since piezoelectric ceramic loudspeakers are highly capacitive in nature, it is desirable to ensure that the amplifier driving it does not become unstable and oscillate at 180° phase shift.

A simple way to do this is to compensate outside of the amplifier feedback loop using a small value series isolation resistor,  $R_{ISOL}$ , as shown above.

The value of the isolation resistor should be low compared to the operating impedance so that losses in that resistor will not materially contribute to overall losses. A good range of values for  $R_{ISOL}$  is from about 2.7  $\Omega$  to 22  $\Omega$ .

The effect of  $R_{ISOL}$  is to improve the gain and phase margin over frequency.

Another reason to add  $R_{ISOL}$  is that it prevents the amplifier from starting up into a load that looks like a short circuit. Initially, the piezoelectric ceramic speaker will appear to be a large, uncharged capacitor, i.e. short circuit.



## ***Advantages of Ceramic Speakers***

- **Ultra-thin profile**
- **Low weight**
- **Low power consumption**
- **Acoustic design is independent of cavity space**
- **No magnetic fields are generated**



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Incorporating ceramic speakers into portable designs provides many benefits:

- Ceramic speakers are much thinner than traditional dynamic speakers. They are 0.7 mm in thickness.
- Ceramic speakers are ultra-light weight. A typical 20 mm multi-layer piezo ceramic speaker weighs approximately 0.44 grams.
- Ceramic speakers are more efficient. They allow the amplifier to dissipate less power due to the capacitive nature of the speaker.
- Since the SPL of the ceramic speaker is dependent on the surface it is mounted on, it is independent of the back spacing a cavity has to offer.
- Unlike moving coil dynamic speakers, piezoelectric ceramic speakers do not require a magnet or coil which eliminates magnetic fields that could interfere with other circuits in a portable design.

## ***Disadvantages of Ceramic Speakers***

- **Require high driving voltages**
- **Poor low-frequency performance**



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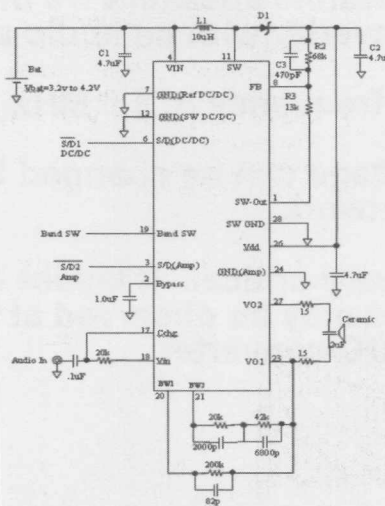


Taiyo Yuden's ceramic speakers require approximately 15Vp-p for acceptable sound pressure level (SPL). Depending upon the battery voltage available in the system, a step-up voltage converter and regulator will be needed to achieve these higher voltages.

## ***Switching Regulator (DC-DC) Converter***

- To drive ceramic speakers we integrated a DC-DC converter with an audio amplifier
- Switching frequency of 1.6 MHz
- Output voltage can be changed by external resistor network
- Layout is very critical. If layout is incorrect oscillations may be observed at the output of the DC-DC converter

## LM4961 - Audio Amp with DC-DC Converter for Ceramic Speakers

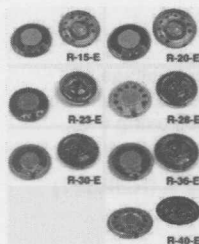


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The LM4961 is an audio power amplifier primarily designed for driving a ceramic speaker for applications in cell phones and PDAs. It integrates a boost converter, with variable output voltage, and an audio power amplifier. It is capable of driving 15Vp-p in BTL mode in to 2  $\mu$ F+ 30 Ohms load with less than 1% distortion (THD+N) from a 3.2 VDC power supply.

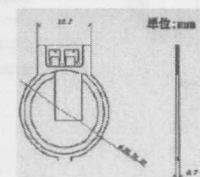
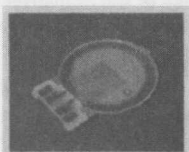
## LM4961 - Audio Amp with DC-DC Converter for Ceramic Speakers



- LM4961 = LM2731 + LM4951
- Designed for ceramic speakers
  - Supply voltage  $V_{dd} = 3.0V - 5V$
  - Amplifier voltage  $V_{amp} = 2.7V - 9V$
- Output voltage swing,  $V_{out} = 15V_{p-p}$  for  $V_{amp} = 7.5V$
- Band SW feature
- Typical application –
  - Cell Phones
  - PDAs
  - Portable consumer products



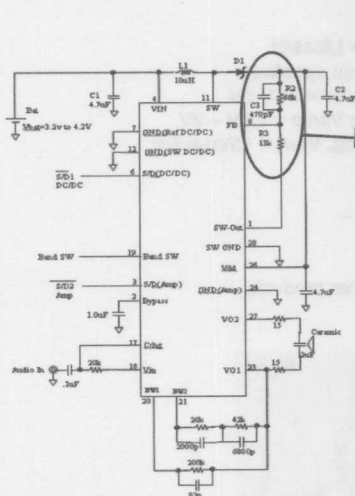
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## Changing the Output Voltage of a DC-DC Converter



• The output voltage of the DC-DC converter can be changed using the following equation:

$$V_{DD} = V_{FB} \times (R2/R3 + 1)$$

$$*V_{FB} = 1.23V$$

• A feed-forward capacitor C3 is required for stability. Adding this capacitor puts a zero in the loop response of the converter. C3 can be calculated using the following equation:

$$C3 = 1 / (2 \times \pi \times R2 \times f_z)$$

\*The recommended frequency for the zero  $f_z$  is approximately 6kHz.

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## **Band Switch Feature**

**The band SW feature allows the customer to use a ceramic speaker for BOTH receiver and ringer modes**

- **Band SW pin low for receiver mode**
  - DC-DC converter disabled
  - Amplifier voltage =  $V_{dd} - \text{Schottkey diode voltage drop}$
  - Changes externally configurable gain select to BW1
- **Band SW pin high for ringer mode - for hands free/ ringer mode**
  - DC-DC converter enabled
  - Amplifier voltage = output of DC-DC converter (7.5V with typical applications circuit configuration)
  - Changes externally configurable gain select to BW2 (can be configured for high gain)

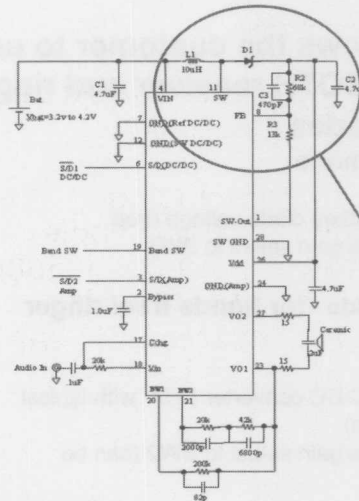


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The LM4961 features a band-switch function which allows the user to use one amplifier for both receiver (earpiece) mode and ringer/loudspeaker mode. When a logic high (VDD) is applied to the band SW pin (pin 19) the amplifier is in ringer mode. This enables the boost converter and sets the externally configurable closed-loop gain selection to BW1. If the band SW pin has a logic low (GND) applied to its terminal, then the device is in the receiver mode. In this mode the boost converter is disabled and the gain selection is switched to BW2. This allows the amplifier to be powered directly from the battery minus the voltage drop across the Schottky diode.

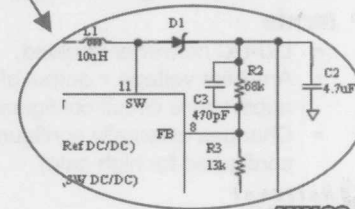
## Importance of PCB Layout



Layout is very critical. If layout is incorrect oscillations at the output of the DC-DC converter may be observed.

- Traces Between L1, D1 and C2 should be extremely short, parasitic trace inductance in series with these components will increase noise and ringing

- Feedback components R2, R3, and C3 MUST be kept close to the FB pin of U1. This trace should be no more than 0.25 in – 0.5 in from FB pin of device



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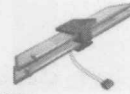


## External Capacitors

- Ultra-low ESR ceramic capacitors should be used for any high-frequency switching converter
- Ceramic capacitors will reduce ringing, switching losses, and output voltage ripple
- Typical aluminum electrolytics are not suitable for switching frequencies above 500 kHz
- An output capacitor with excessive ESR can reduce phase margin and cause instability

## What is a DMA?

### DMA – Distributed Mode Actuator



A DMA consists of one or more bimorph beams of piezo crystal layers connected at a common stub (referred to as veins) which forms the panel forcing point

- A bimorph beam consists of a metal shim sandwiched between two thin piezo ceramic layers
- A single layer DMA has a single piezo ceramic layer, which causes DMAs to have low capacitance (~200 nF) and high driving voltages (16 Vrms)
- A multi-layer DMA has piezo ceramic layers which consist of three (or five) sub-layers. This allows the DMA to have higher capacitance (~800 nF), and lower driving voltages (10 Vrms)
- Applying a voltage across them alters their length, allowing them to be used as actuators on a flat panel
- DMAs force and velocity can be independently varied across a wide range by altering the length, width, and thickness of the piezo crystal beam, and by adding further beams, if necessary



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As mentioned above, a DMA's force and velocity can be independently varied by altering the length, width and thickness of its beam or by adding further beams, if necessary. Therefore, its mechanical impedance can be matched to the panel in such a way as to maximize frequency bandwidth response. In practical use and for optimal performance, DMAs would be ideally matched to the panel material to which they are attached.

The panel can be made from a wide array of materials such as plastic, glass, cardboard paper, etc. NXT sound offers some packaged solutions using DMAs and "SoundVu" panels.

These DMAs, like ceramic speakers, do not require a magnet or a coil. This eliminates any magnetic fields that would be normally generated by moving coil speakers.

## **Benefits of DMAs**

- Battery to acoustic power of DMA applications in mobile devices can be more than tenfold that of conventional speaker systems
- Multi-layer DMAs have high capacitance values (typically over 800 nF) and lower driving voltages (10 Vrms max), as opposed to single layer DMAs which have lower capacitances (~200 nF) and require higher driving voltage (16 Vrms max)
- System's surface becomes the speaker, therefore making it ideal for portable applications



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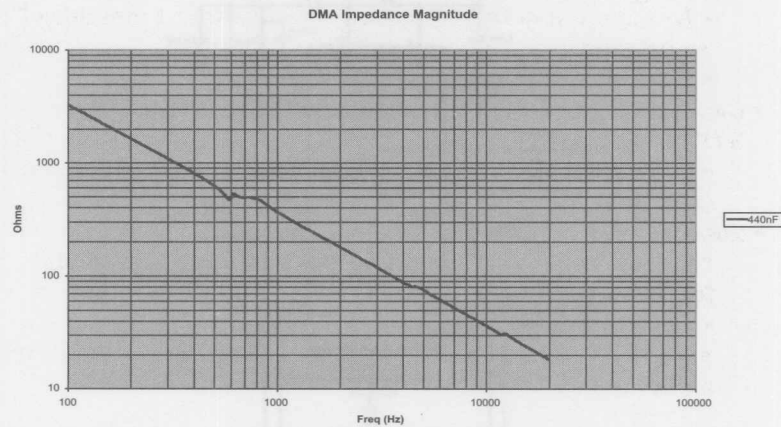


## **Electrical Characteristics of DMAs**

- Full audio frequency range 20 Hz to 20 kHz
- Small lightweight solution
  - A single-beam DMA is typically only about 1 mm thick with typical weight being less than 2 grams
  - Product surface becomes the speaker
- Capacitive load (~800 nF) as opposed to a resistive 8 Ohm load
  - Load impedance varies over frequency (low impedance @ high freq)
- Load voltage
  - ~16 Vrms for single-layer DMAs or ~10 Vrms for multi-layer DMAs
  - Therefore, amplifier supply voltage = 15 V
  - A DC-DC converter is needed to supply 15 V to the audio amplifier



## Load Impedance of DMAs



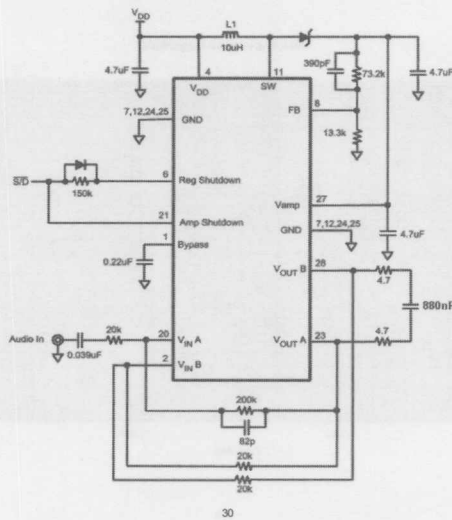
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A representative impedance vs frequency curve of a multi-layer Dynamic Mode Actuator (DMA) is shown above.

## LM4960 Mono Audio Amp with Switching Regulator

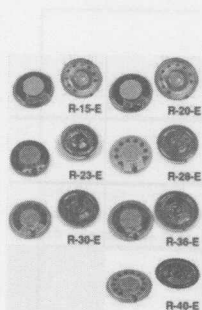


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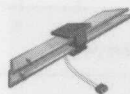
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The LM4960 utilizes a switching regulator to drive a dual audio power amplifier. It delivers 24 V(p-p) mono-BTL to a ceramic speaker with less than 1.0% THD+N while operating on a 3.0 V power supply. The LM4960's switching regulator is a current-mode boost converter operating at a fixed frequency of 1.6 MHz.

## LM4960 Mono Audio Amp with Switching Regulator



- LM4960 = LM2731 + LM4950
- Supply ranges
  - Supply voltage  $V_{dd} = 2.7V$  to  $7V$
  - Audio amp supply  $V_{amp} = 9.6V$  to  $16V$
- DC-DC converter allows up to **15V output**
- Output voltage swing,  $V_{out} = 10V_{rms}$  ( $28V_{pp}$ ) for  $V_{amp} = 15V$
- Designed to drive
  - Multi-layer DMAs
- Typical application –
  - Cellphones
  - PDAs
  - Portable consumer products

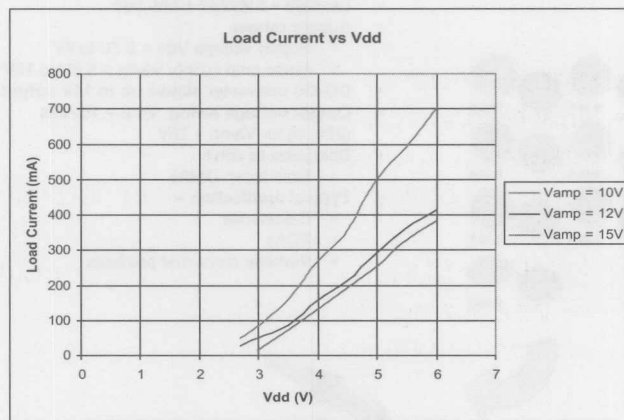


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## LM4960 Output Current Capability



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A graph of load current vs supply voltage for different regulator output voltages (Vamp) is shown above.



## ***Trends Driving Audio***

- Higher efficiency
- New technologies (new speaker variations)
- Integrated audio subsystems
- Audio becoming “differentiator” in portable products
  - MP3, FM stereo, 3D stereo ring sounds
  - Maximizing battery life
  - Smaller / thinner / lighter



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## ***Stereo Loudspeakers in Handsets***

- Provides an additional 6 dB of output level for the same mono audio input level
- Output noise levels are not increased by 6 dB, which translates to better SNR performance for the listener
- High-quality stereo FM radio and MP3 playback capability have become a part of the standard feature set for handsets



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## ***Why Use National 3D Enhancement?***

- Handset size is limited
- Placement of speakers is limited to handset size
- Stereo speakers placed too close to another have the effect of producing a stereo output with a mono image (poor stereo channel separation)
- National 3D enhancement widens the image of the stereo output and improves the stereo channel separation



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Stereo enhancement refers to processing stereophonic music or sound in such a way as to add spaciousness to the stereo sound field. The purpose of stereo enhancement is to widen the stereo sound field, thereby immersing the listener in a cleaner, richer sound experience, significantly improving the quality, depth, and feel of the music played. From a practical point of view, stereo enhancement is intended to spread the stereo field into a 180° arc in front of the listener.

## **Types of Stereo Enhancement**

- **Volume or intensity**
- **Distance or delay**
- **Phase shifting**



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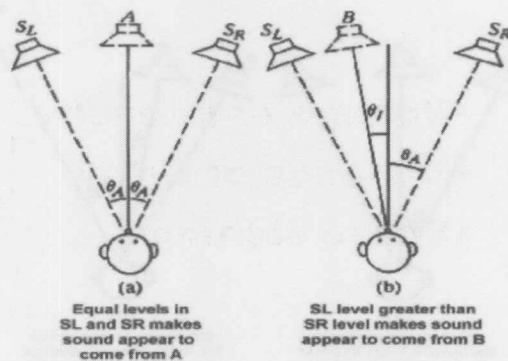


There are many techniques for stereo enhancement. Most of them are variations on a common technique described in this early patent:

### *US PATENT 4,910,778 – DESCRIPTION:*

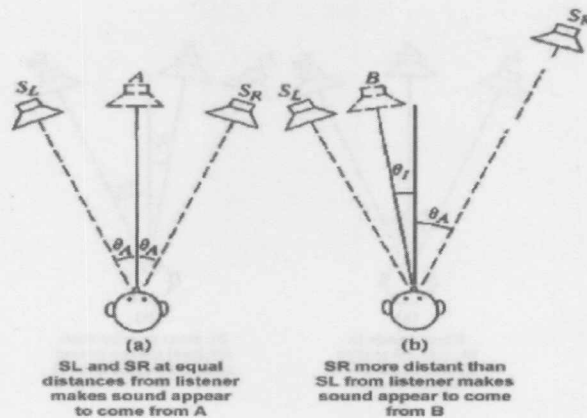
*The enhancement processor disclosed herein includes left and right channels through which the components of the stereo signal are fed, and a side channel that receives a difference signal derived from the main left and right channel signals. The side channel difference signal is shifted in quadrature, (e.g. + or - 90°) relative to the main channels of the processor, adjusted by a variable gain control (G1), low pass filtered and added back into the main left and right channels prior to the stereo outputs. Further enhancement is achieved in the processor by combining with the above effect, a gain (G2) adjusted anti-phase cross-feed widening characteristic that compensates for some undesired image alteration resulting from the quadrature shifted side channel.*

## Intensity or Volume Stereo Enhancement



One way to alter the apparent location of a sound within a stereo field is to alter the intensity or volume of one channel. The sound will appear to come from a point closer to the loudest channel.

## Delay Stereo Enhancement



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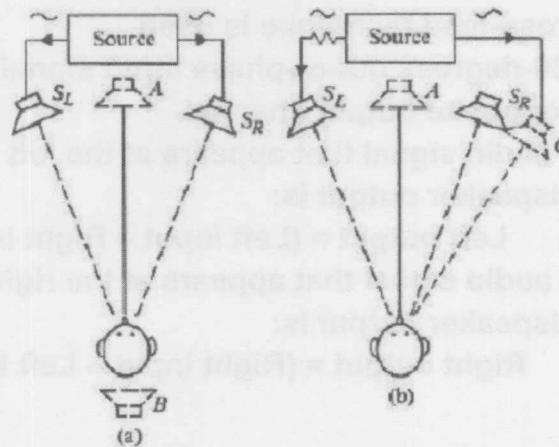
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Another way to alter the apparent location of a sound source in a stereo field is to delay the arrival of the signal in one channel. In the example above, the delay is introduced by moving the SR loudspeaker further from the listener.

Instead of locating loudspeakers at different distances, a very simple method to alter the apparent location of a sound in the stereo field is to delay one channel relative to the other one by about 10 mSec.

If the delay is on the right channel, the stereo image will appear to be more toward the left. Generally, gain would have to be added to the delayed right channel, otherwise, the sound will have appeared to move further away as well as to the left.

## Phase Shifting Stereo Enhancement



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Another method to widen the stereo field involves out-of-phase signals in one channel. For example, as shown in (a) above, when the  $S_L$  &  $S_R$  loudspeaker signals are in phase, the sound will appear to come from location A and spread out the non-centered sounds. But if the phase is reversed in one channel, the sound will appear to come from location B, behind the listener. In some cases, the listener may perceive the sound as coming from inside his head. Further changes will occur if one channel's intensity is significantly reduced. As shown in (b) above, the sound will shift from location B to location C beyond the right speaker  $S_R$  if the left channel intensity is greatly reduced.

## **How Does National 3D Enhancement Work in the LM4857?**

- A cross-feed technique is used
- A 180-degrees out-of-phase input signal appears at the opposite output channel
- The audio signal that appears at the left loudspeaker output is:

$$\text{Left output} = (\text{Left input} - \text{Right input})$$

- The audio signal that appears at the right loudspeaker output is:

$$\text{Right output} = (\text{Right input} - \text{Left input})$$



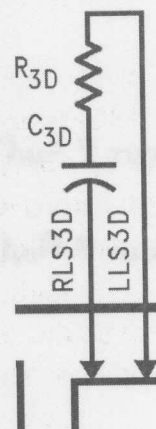
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## How Does National 3D Enhancement Work in the LM4857?

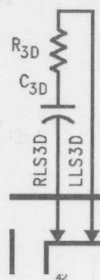
- Two external components  $R_{3D}$  and  $C_{3D}$  complete the cross-feed network of the National 3D enhancement block



## 3D Effect Equation

- $L_{OUT} = L_{IN}(1 + (20k / R_{3D})) - R_{IN}(10k / R_{3D})$

- $R_{OUT} = R_{IN}(1 + (20k / R_{3D})) - L_{IN}(10k / R_{3D})$



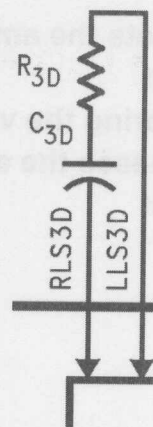
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## How Does National 3D Enhancement Work in the LM4857?

- $R_{3D}$  and  $C_{3D}$  set the lower cutoff frequency at which the 3D effect starts to occur

$$f_{3D(-3dB)} = 1 / 2\pi(R_{3D})(C_{3D})$$



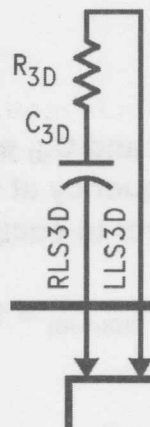
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## How Does National 3D Enhancement Work in the LM4857?

- $R_{3D}$  sets the amount of the 3D effect
- Lowering the value of  $R_{3D}$  increases the amount of 3D effect



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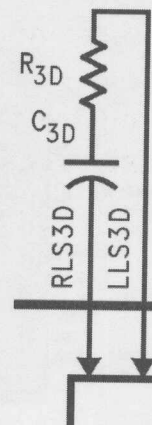
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## How Does National 3D Enhancement Work in the LM4857?

- $R_{3D}$  increases the output signal by a multiplication factor of:

$$(1 + 20k / R_{3D})$$

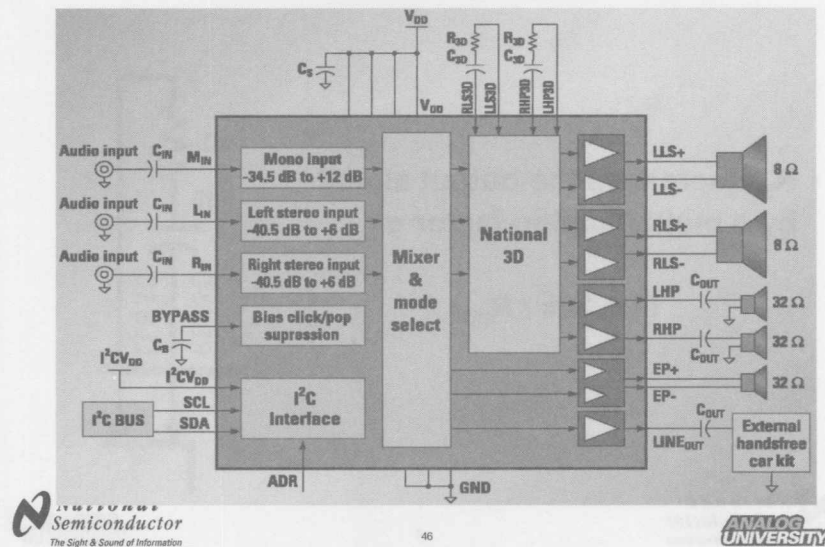


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## LM4857 Audio Subsystem



The LM4857 is an integrated audio subsystem designed for stereo cell phone applications. Operating on a 3.3 V supply, it combines a stereo speaker amplifier delivering 495 mW per channel into an 8 Ω load, a stereo headphone amplifier delivering 33 mW per channel into a 32 Ω load, a mono earpiece amplifier delivering 43 mW into a 32 Ω load, and a line output for an external powered hands-free speaker. It integrates the audio amplifiers, volume control, mixer, power management control, and National 3D enhancement all into a single package. In addition, the LM4857 routes and mixes the stereo and mono inputs into 16 distinct output modes. The LM4857 is controlled through an I<sup>2</sup>C compatible interface. Other features include an ultra-low current shutdown mode and thermal shutdown protection.

## **LM4857 Stereo Audio Subsystem**

- Enhances user experience
  - Stereo enhanced MP3, polyphonic ring sounds
- High level of analog integration
  - Independent stereo enhancement
    - Headphones, stereo speakers
  - Earpiece, car kit support
  - Stereo headphones, stereo ringer
  - Eliminates 17 external components
- Audio console functionality – 16 modes
- Miniature packaging – micro SMD

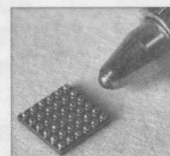



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## ***LM4857 Stereo Cell Phone Audio Subsystem with 3D Enhancement***

- 495 mW @ 3.3V,  $R_L = 8\Omega$  1.0% THD
- 33mW @ 3.3V,  $R_L = 32\Omega$  1% THD
- Line out for hands-free car kit
- Separate Stereo & Mono volume controls
- National 3D enhancement
- I<sup>2</sup>C compatible control interface
- 16 Output Modes
- Available in micro SMD and LLP<sup>®</sup> packages
- Targeted for stereo phones with FM radio/MP3 playback and portable gaming systems



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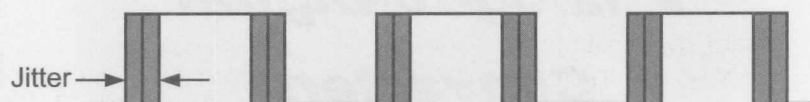


## ***Analog-to-Digital Converters***

At one time we did not worry about jitter with analog-to-digital converters because it was not a real issue at the frequencies that ADCs could handle. Today's ADCs can accept and are used with input frequencies in the hundreds of Megahertz and beyond 1 GHz for digitization. Sensitivity to jitter increases with higher signal frequency and ADC resolution.

## ***What is Jitter?***

- **Jitter** – the cycle-to-cycle variation in the signal edge relative to another edge



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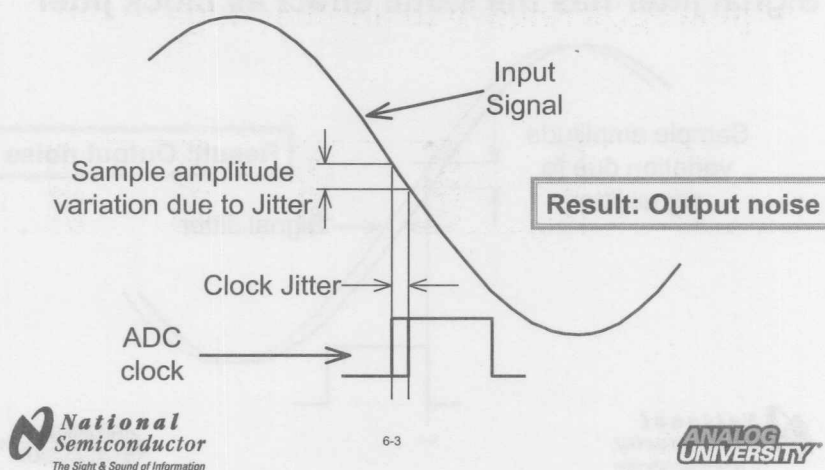
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Jitter is defined here as the cycle-to-cycle variation in the edge of a signal.

# Clock Jitter

**Jitter: cycle-to-cycle variation in timing**

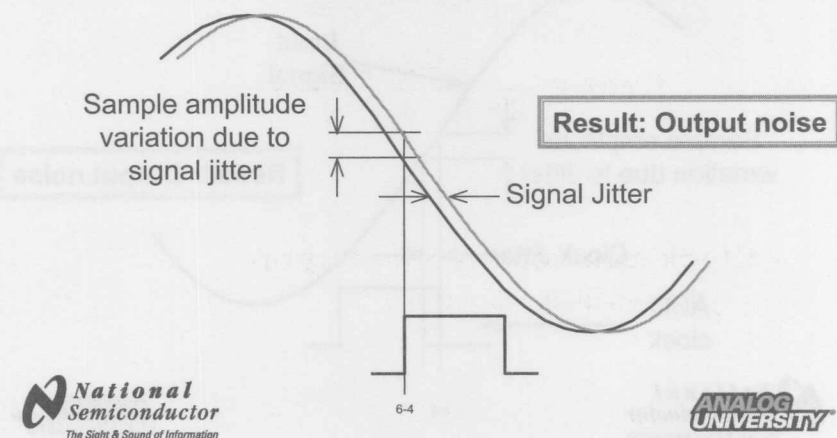


Because jitter in the ADC clock relative to the input signal means that there is a variation in the time a signal is sampled, there is variation in the sampled signal level. If we try to sample the same point in a waveform at every cycle of that waveform we may sample levels between due to the presence of jitter. For example, 1.14 V to 1.15 V, or a 10 mV spread in this case. This means there is 10 mV of noise at the output. With 6- or 8-bit resolution this might not be too bad, but at higher resolutions this can be significant.

The effect of jitter is more easily seen at higher resolutions (digital word widths).

# Signal Jitter

Signal jitter has the same effect as clock jitter



When considering jitter in ADC applications, we generally think of clock jitter. However, jitter that is added to the input signal has the same effect as jitter in the sample clock. The problem lies in the clock jitter relative to the signal jitter.

## ***High-Speed ADC Clock Considerations***

- Maximum allowable jitter to prevent noise degradation:

$$t_{j,max} = \frac{V_{IN(P-P)}}{2^{(n+1)} * V_{FS} * \pi * f_{in}}$$

- Clock rate has no effect upon jitter-induced noise



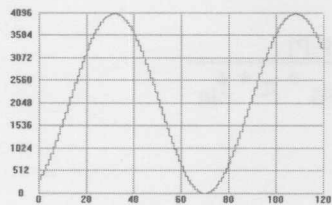
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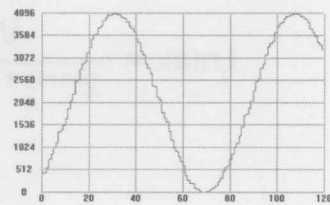
Jitter in the sampling clock or in the input waveform (actually, the jitter between the two) results in decreased noise performance, as we will see shortly. The maximum jitter for all sources is as shown if we are to prevent it from affecting performance. Jitter is a prime source of noise with digitized high-frequency signals. Note that sample rate does not enter this formula.

Most people use a  $2^n$  factor rather than the  $2^{(n+1)}$  shown here, but that would limit the noise to one LSB. Using a factor of  $2^{(n+1)}$ , as shown here, limits the noise to  $\frac{1}{2}$  LSB, which means, for all practical purposes, no noise.

## Effects of Jitter



Sampled with "clean" Clock



Sampled with Jittery Clock

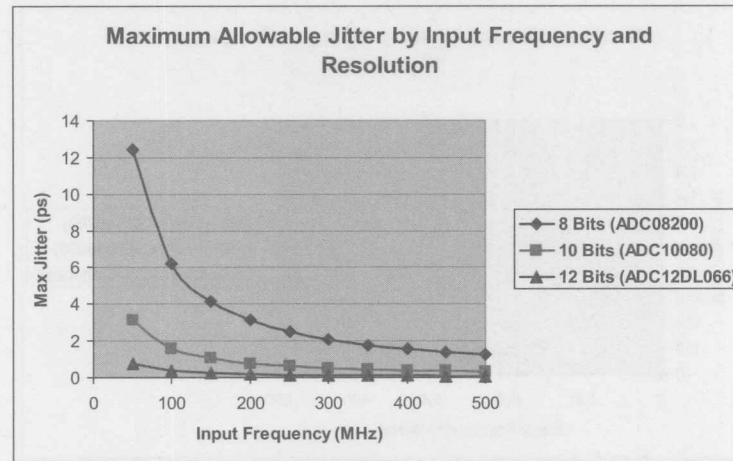


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These plots from National's WaveVision software show the effects of excessive clock jitter. The noise on the signal is apparent.

## Maximum Jitter



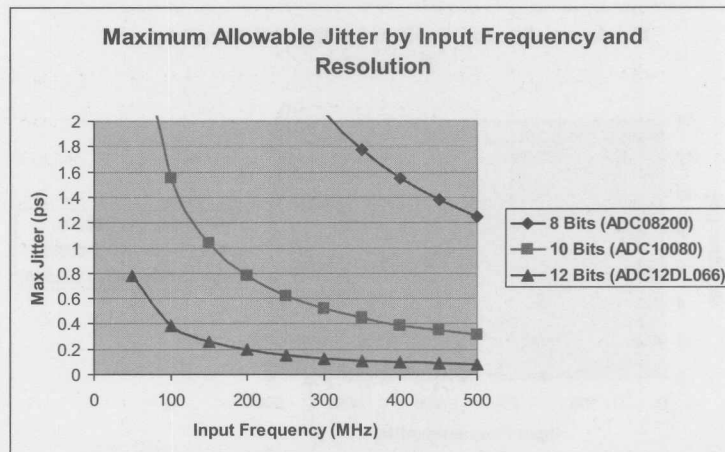
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The maximum jitter tolerable without suffering a degradation in SNR is determined by the resolution of the A/D converter and the frequency of the input signal, as well as the signal amplitude relative to full scale. Again, the sample rate has no effect upon the maximum allowable jitter to prevent noise degradation.

## maximum jitter(4)

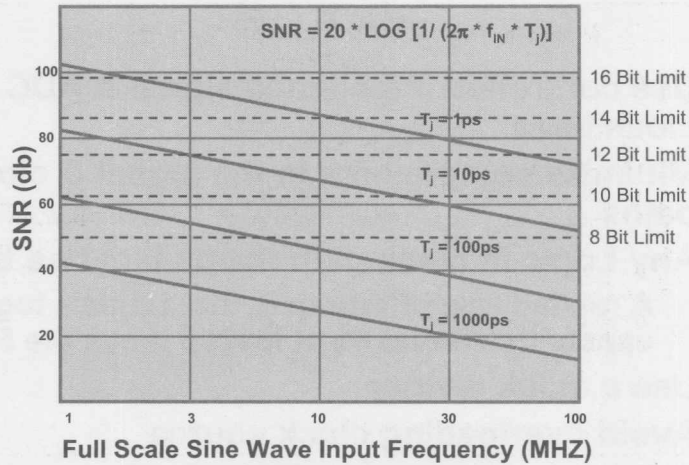


This is the same as the previous slide with the vertical scale expanded.

It seems that avoiding noise-induced jitter is an impossible task at very high input frequencies and high resolutions. Careful selection of the clock source and how it is presented to the ADC, as well as proper attention to design and layout, will go a long way toward maximizing circuit performance.



## Jitter Effect Upon SNR



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This graph shows the relationship between ADC input frequency, SNR and Clock Jitter. Of course, SNR will never be better than that indicated by the ADC resolution (Best SNR =  $20 * \log(2n) + 1.76$  dB, where "n" is ADC resolution). Therefore, the best theoretical SNR for an 8-bit ADC is 49.9 dB and the best theoretical SNR for a 16-bit ADC is 98 dB. The theoretical SNR limit by resolution is shown with the dashed lines here.

## ***Minimizing Jitter***

- Use controlled impedance signal & ADC clock lines
- Minimize components in the signal & clock paths
- Any Logic in clock path needs fast rise time.
  - A related rule of thumb is that Logic's toggle capability should be at least 5 times the  $F_{IN}$
- Use a clock divider
- Avoid overloading clock source



6-10



Full attention to these guidelines will help minimize noise problems.

Using a controlled impedance clock line implies one source driving a single destination.

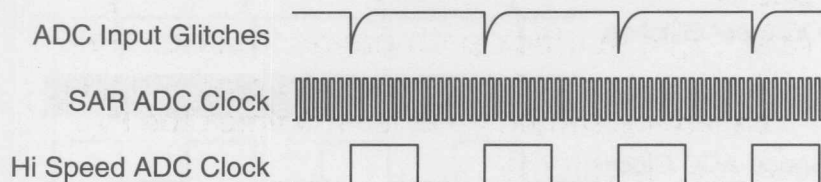
Logic components tend to add jitter to the signal unless its toggle capability is significantly higher than the used toggle rate.

Starting with a high frequency clock and dividing it down (using circuitry capable of toggle rates much higher than the starting frequency) will reduce clock jitter, if done carefully.

Overloading a clock source can add a lot of jitter to the clock signal. A high capacitive load on a crystal-based overtone oscillator can cause it to operate in its fundamental mode rather than its intended overtone mode.

## ***ADC Input Glitches – Passive Drive***

- ADC input glitches are caused by sampling action
- It is not necessary to eliminate the glitches
- Input needs to settle before sampling switch opens



Sample switch closes on rise of clock,  
causing input glitches

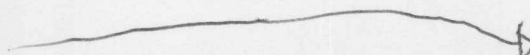
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6-11

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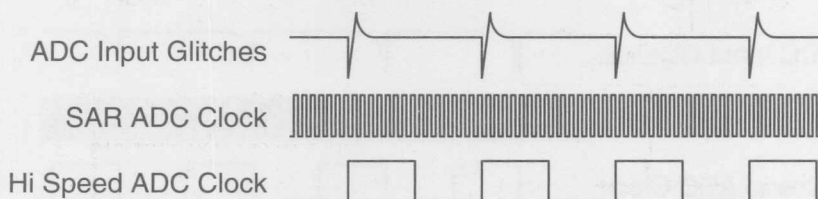
A look at the sampling ADC input will reveal pulses at the ADC sample rate. These pulses are caused by the recharging of the ADC sampling capacitor at the start of each conversion cycle. The user should not attempt to filter out these pulses, which are completely normal. However, the pulses should settle out before the end of the sampling time, which is generally specified in the data sheet.

In the case of high-speed ADCs with a sample rate equal to the ADC clock rate, the sampling time is usually either the clock low time (when the sampling edge is the rise of the ADC clock) or the clock high time (when the sampling edge is the fall of the ADC clock). SAR (Successive Approximation Register) based ADCs usually sample for more than one clock period.

 Wavevision

## ADC Input Glitches – Amplifier Drive

- ADC input glitches are caused by sampling action
- It is not necessary to eliminate the glitches
- Input needs to settle before sampling switch opens



Sample switch closes on rise of clock,  
causing input glitches

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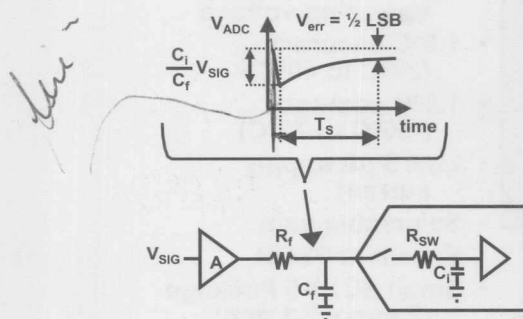
6-12

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If a feedback amplifier (operational amplifier) is used to drive the ADC input, there may be overshoot as the amplifier over corrects for the pulse. Again, there should be no attempt to filter out these pulses, but they should settle out before the end of the sampling time.

## ADC Sampling Filter

- Input needs to settle before sampling switch opens
- Sampling filter isolates capacitance from amplifier while allowing input to settle



$$V_{ADC} = V_{SIG} - V_{err}$$

$$\text{where } V_{err} = \frac{C_i}{C_f} * FSR * e^{-(t/\tau)}$$

$$t = T_s, \tau = R_f C_f$$

$$V_{err} < \frac{1}{2} \text{ LSB}$$

$$C_f \geq 10 \cdot C_i$$

$$R_f \leq \frac{T_s}{10 \cdot C_f \cdot \ln[10 \cdot 2^{-(n+1)}]}$$

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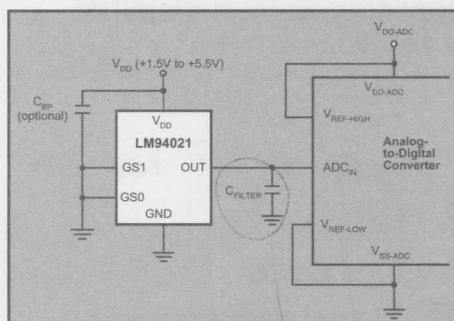
6-13

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Standard practice when driving the input of sampling ADCs is to isolate the op-amp output from the ADC input with a small resistor and a capacitor. The reason for this is allow faster settling of the ADC input to ensure that it has settled before the ADC sampling switch opens. Additionally, some Successive Approximation Register (SAR) ADCs can have a large input capacitance that might bring instability to the driving amplifier. The resistor between the amplifier output and the ADC input will isolate the ADC input capacitance from the amplifier output and improve loop stability. The RC time constant, including the ADC input capacitance, should be such that the RC cutoff frequency is approximately the same as the sample rate of the ADC. That is,  $f_s = 1/(2\pi RC)$ .

Refer to the op-amp datasheet for specific information when driving capacitive loads.

## Example: Analog Temperature Sensing with LM94021



- Very linear temperature to output transfer function
- Low 1.5 V minimum operating voltage
- 1.5°C accuracy (20°C to 40°C)
- 1.8°C accuracy (-50°C to 70°C)
- Low 9  $\mu$ A supply current
- Selectable gain
- Excellent PSRR
- Small SC70-5 Package (2 mm x 2.1 mm)

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6-14

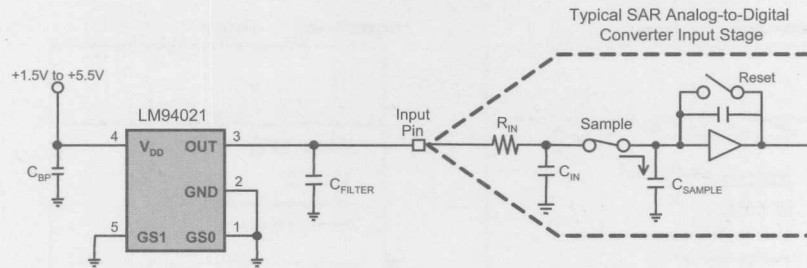
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An analog temperature sensor can perform direct analog compensation for a circuit or device. For example, an analog temperature sensor like the LM94021, LM20, or LM61, can be used in a circuit designed to control the frequency of an oscillator, compensating for frequency shift due to temperature. This would be a temperature compensated crystal oscillator circuit.

Another method of using an analog temperature sensor is to feed its output directly into an analog-to-digital converter, which is sometimes embedded within a processor or ASIC. The binary temperature data can then be used by the processor or ASIC to take appropriate compensating action, such as reducing the bias current to a power amplifier.

The LM94021 analog temperature sensor operates with a supply voltage as low as 1.5 V and consumes only 9  $\mu$ A (typical), making it ideal for today's low-power systems. Configuring the digital input pins GS1 and GS0 selects four possible gains: -5.5 mV/°C, -8.2 mV/°C, -10.9 mV/°C, or -13.9 mV/°C. This allows the system to be optimized for sensitivity and temperature range. Also, a host processor can drive the input pins and monitor the output for in-system testing. The excellent noise rejection reduces component count. The LM94021 is capable of driving 1100 pF of capacitive load without the need for any other components at the output. These reductions in component count, along with the small package, translate into a savings in board area and cost.

# Interfacing Temperature Sensor to an ADC Input



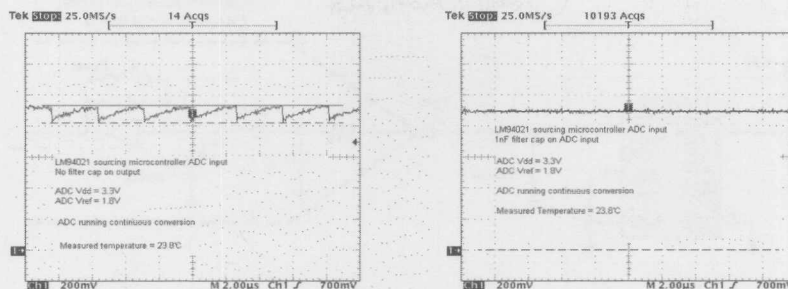
6-15



Most CMOS analog-to-digital converters (ADC) found in microcontrollers and ASICs, as well as many stand-alone ADCs, have a sampled data comparator input structure. When sampling, the sample capacitor ( $C_{\text{SAMPLE}}$ ) charges to the voltage present on the analog input. This charging requires current from the source. As a result, the source output stage is heavily loaded, causing transient spikes on the signal, as we have just seen. A filter capacitor ( $C_{\text{FILTER}}$ ) is commonly used at the input of the ADC. This capacitor stores charge for use during sampling, keeping the output stable by filtering out the transient spikes.



# Without an Input Filter Cap



*The "Measured Temperature" is measured with a separate sensor.*



6-16

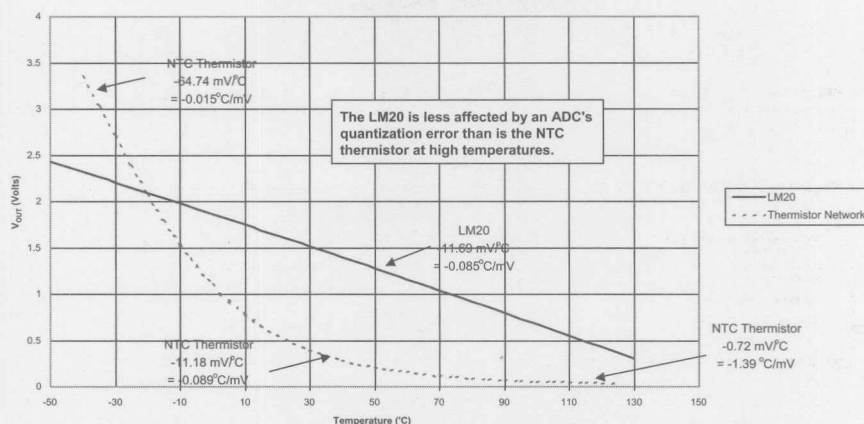


These two scope photos demonstrate (1) the transient loads placed on the source when the ADC's sampling capacitor is charging and (2) the stability achieved by placing a filter capacitor at the input to the ADC. The capacitor is needed when the sampling rate is too fast to allow the temperature sensor output (ADC input) to stabilize. When the sensor is a low-power device, as with the LM94021, it may not produce enough output current to settle before the sample is taken. The addition of a filter capacitor will improve accuracy. The size of this capacitor will depend upon the size of the sample capacitor (in this case, the ADC sampling capacitor was approximately 50 pF) and also upon the sampling frequency. Generally, the filter capacitor value should be about 10 to 20 times the ADC sample capacitor value. Care must be taken to ensure that the sample frequency is matched to the maximum source current of the sensor so that the filter capacitor remains charged to the appropriate level. As you can see in the first image, the output gets pulled low as the sample capacitor starts to charge. If the sample rate is faster than the time in which the capacitor can be recharged, that capacitor would still be charging and not settled when the next sample occurs. The second image shows the benefit of adding a 1nF filter capacitor at the ADC's input. The result is a stable DC voltage which is proportional to temperature.

Note also that the "Measured Temperature" indicated here is the temperature measured with a separate sensor.



## Transfer Function Comparison LM20 vs. a Thermistor



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As we have seen, the output of an analog temperature sensor is often fed into an ADC. Every ADC has a quantization error associated with it. The higher the resolution of the ADC (the more bits it has), the smaller the quantization error. When digitizing the output of an analog temperature sensor, this quantization error translates directly into a temperature-reading error -- the higher the quantization error (the lower the ADC resolution), the higher the temperature-reading error.

The slope of the temperature sensor's transfer function (change in voltage per change in temperature) determines how severe of an impact the ADC error will have on the temperature measurement. Let's say that an 8-bit ADC has a reference of 5V so that each LSB is equal to about 20 mV. The LM20, as an example, has a slope of 11.69 mV/ $^{\circ}\text{C}$ . This is equivalent to  $-0.085^{\circ}\text{C}/\text{mV}$ . This means that one LSB of quantization error would result in a maximum  $(0.085^{\circ}\text{C}/\text{mV} * 20 \text{ mV}) = 1.7^{\circ}\text{C}$  error.

Consider now that the NTC thermistor has a slope of  $-64.7 \text{ mV}/^{\circ}\text{C}$  at  $-35^{\circ}\text{C}$ . Its temperature error due to quantization would be  $0.30^{\circ}\text{C}$  error at this cold temperature. However, at  $120^{\circ}\text{C}$  the thermistor has a slope of  $-1.39^{\circ}\text{C}/\text{mV}$ . So it would have a digitized temperature error of  $27.8^{\circ}\text{C}$ ! The plot above shows that the LM20 performs better at temperatures above  $35^{\circ}\text{C}$ , the point where the thermistor has approximately the same slope as that of the LM20. Also, the LM94021 has four possible gains, so the quantization error can be managed by simply changing the gain.





## ***Minimizing Noise in Designing with A/D Converters***

1

We know that noise is always an issue. Adding more circuitry usually adds more noise. There are things that can be done, however, to minimize the impact.

## More Components: More Noise

- System SNR is the RSS of SNR of all components in the signal chain
- The worst SNR dominates
- Components with higher SNR have less effect upon overall SNR



$$\text{Overall SNR} = 20 \text{ LOG} \sqrt{10^{\frac{-\text{SNRA1}}{10}} + \dots + 10^{\frac{-\text{SNRAm}}{10}} + 10^{\frac{-\text{SNRADC}}{10}}}$$



7-2



When discussing noise issues, we should note that increasing the number of components in the signal chain will combine in a root of the sum of the squares (RSS) manner. The overall SNR of the system will be determined as indicated here. Note that the first few amplifiers will have the greatest effect. Each additional amplifier will have less effect than the last added one.

## ***dB Loss Table*** ***(All Amplifiers of Equal SNR)***

- Each added amp degrades SNR less than the previous one
- All figures are in dB

# of Amps	Incremental Loss
2	3.01
3	1.76
4	1.25
5	0.97
6	0.79
7	0.67
8	0.56
9	0.46
10	0.38
11	0.31



7-3



This chart indicates the incremental SNR loss with the addition of more amplifiers or other components, all with equal values of SNR. If there are differing SNRs, the component with the worst SNR will dominate, as can be seen with the formula on the previous page.

# Op-Amp Gain Bandwidth

- Closed loop bandwidth must exceed  $R_f C_f$  cutoff

$$f_{cl} \geq \frac{1}{2\pi * \tau} \quad GBW = A_v \times f_{cl}$$

$$GBW \geq - \frac{A_v}{2\pi * \tau} \times \ln \left[ \frac{C_f}{C_i} \times 2^{-(n+1)} \right]$$

$$GBW \geq - \frac{A_v}{2\pi T_s} \times \ln \left[ \frac{C_f}{C_i} \times 2^{-(n+1)} \right]$$



7-4



In order to satisfy ADC settling-time requirements, the driving amplifier must have adequate bandwidth to recharge the filter capacitor,  $C_f$ , before the end of the sampling period. A useful rule of thumb for approximating the required minimum closed-loop bandwidth is found by assuming a first order closed-loop response for the op-amp, which allows the substitution for  $\tau$  as shown above. Solving for  $f_{cl}$  we get:

$$f_{CL} \geq - \frac{1}{2\pi \tau} \times \ln \left[ \frac{C_f}{C_i} \times 2^{-(n+1)} \right]$$

Making the substitution for  $C_f = 10 C_i$  and noting that the gain bandwidth product (GBW), of an op-amp is equal to the closed-loop DC gain times the closed-loop bandwidth, we get the above rule of thumb.

## ***Minimum Amplifier Slew Rate***

- Max slew rate of a sine wave is the first derivative of that signal

$$\frac{dV_{SIG}}{dt} = 2 \times \pi \times \frac{V_{IN(P-P)}}{2} \times f_{IN} = \pi \times V_{IN(P-P)} \times f_{IN}$$



7-5



If the output of the driving amplifier can not slew as fast as the signal demands the amplifier will distort the signal. Thus the minimum slew rate of the amplifier is whatever is required to faithfully reproduce its input signal at the required level to input of the ADC. The maximum slew rate of the signal is the first derivative of the signal at the required amplitude. As noted in the prior sections on op-amp performance characteristics, the minimum amplifier slew rate needs to be five to ten times higher than this value for low distortion.

## ***Be Aware of The Effects of Offsets***

- ADC has zero scale and full scale gain errors
- Amplifiers have offset ( $V_{OS}$ ) and gain errors
- These errors are additive
- ADCs have zero scale and gain error tempcos
- Amplifiers have offset tempco (drift)
- These tempcos are additive
- Most important in DC coupled applications
- Allowable tolerance depends upon  
system requirements



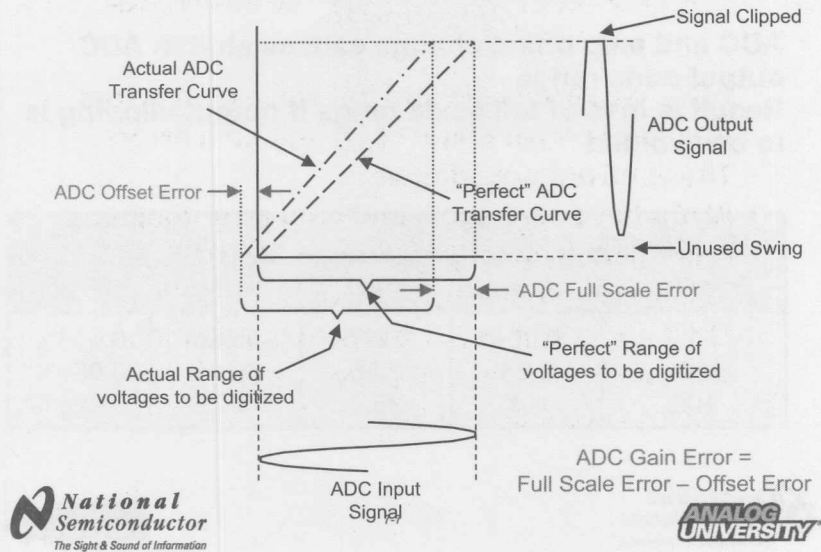
7-6



Here we see some important considerations regarding offset and gain errors in the ADC and amplifiers that drive the ADC. Offset and gain errors have temperature coefficients that are additive. How much these errors can be tolerated is determined by system requirements.



## ADC Offset and Gain Errors



Here we see the effects of offset and gain errors. Of course, any amplifier offset error will add to the offset error of the ADC, as will any gain error.

- ADC and amp offset change causes shift in ADC output code range
- Result is loss of full scale range if output clipping is to be avoided

$V_{OS}$ Drift, $\mu\text{V}/^\circ\text{C}$	LSB Shift over $-40^\circ\text{C}$ to $+85^\circ\text{C}$ (FSR = 2V)			
	10 Bits	12 Bits	16 Bits	FSR Loss
1	0.064	0.256	4.096	0.006%
10	0.64	2.56	40.96	0.063%
100	6.4	25.6	409.6	0.625%



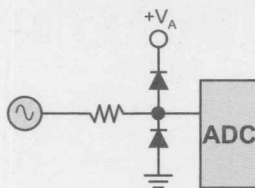
7-8



If we are to avoid clipping of the ADC output, we must reduce the input swing to allow for worst-case offset and gain errors and their drifts. This means a loss of input dynamic range and a resulting loss of SNR performance. However, this is not the only problem with offset and gain errors.

## ***Input Overdrive***

- Driving the ADC input beyond the supply rails can cause latch-up
- Potential problem when using different supplies for ADC and driving device



Input Protection

7-9

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If the input to any device, ADC or otherwise, is driven far enough beyond the supply rails for that device, the result can be a latch-up of that device. A hard latch-up can be destructive, but more often there is a soft latch-up, whereby the device does not work properly or may not function as an ADC at all.

Examples of potential problems include driving a single +5V supply ADC with an amplifier that is powered from  $\pm 5V$ , from  $\pm 12V$  or +12V, or even from a separate +5V supply source from the ADC's power source.

Protecting the inputs with a resistor and two diodes, as shown here, is an effective way of protecting most ADC inputs. However, this may not be adequate for some devices, particularly older devices.



7-10



## ***Signal Integrity and PCB Layout Considerations***

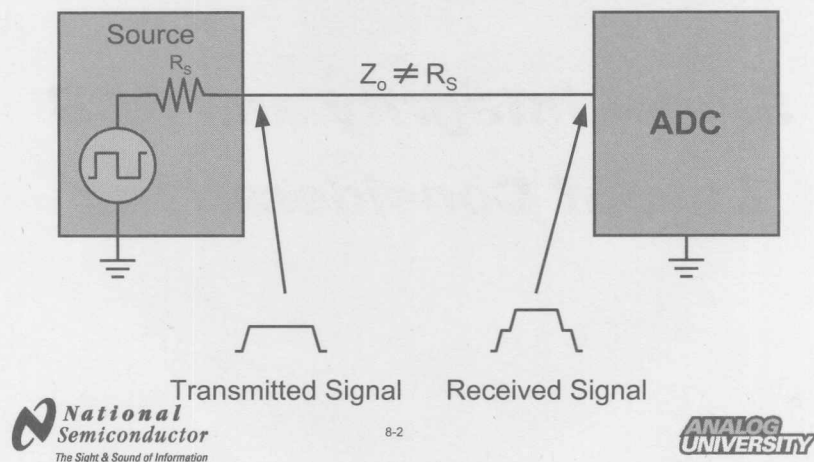
Signal integrity has become a popular topic in light of the very high edge rates that have resulted from high-frequency digital communications. Working with today's high-speed digital signals has meant that digital designers must be concerned with signal integrity. Signals associated with today's ADCs are no exception.

Actually, even today's lower-speed ADCs can be affected because digital circuitry today, even with low toggle rates, tends to have very fast edge rates (rise and fall times). It is these edge rates that require attention to signal integrity, not just the toggle rate.

Layout considerations take us into what might be a whole new world, a "Twilight Zone", if you will, and is very much concerned with signal integrity. We will try to simplify these considerations and give you a couple of examples of typical problems in this area.

# Signal Integrity Problem

This is NOT a controlled impedance line

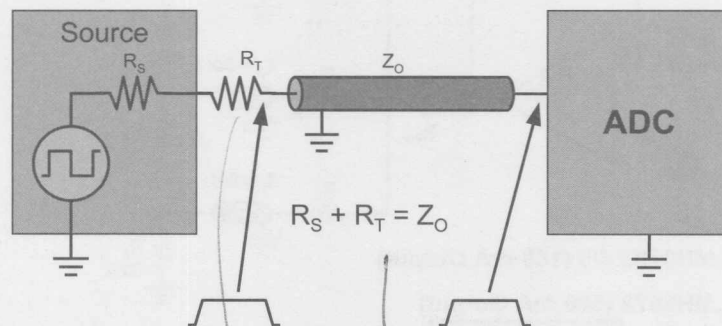


All interconnecting lines are transmission lines. If the transmission-line characteristic impedance ( $Z_0$ ) is not matched to the signal-source impedance or the signal-receiver input impedance, there will be reflections on the line that can cause distortion and even amplitude doubling of the signal. This loss of signal integrity could cause any number of problems in a system.

In the case of the ADC clock line, this mismatch can result in noise, missing codes, or erratic operation.

# Maintaining Signal Integrity

This IS a controlled impedance line



Treat the connection as a transmission line

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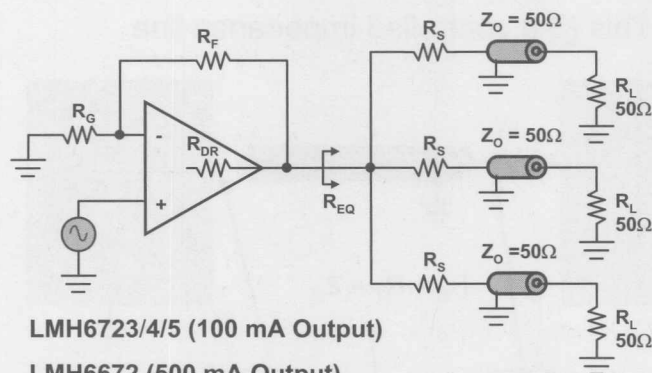
8-3

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Adding a series terminating resistor such that its value plus the signal-source impedance equals the characteristic impedance of the transmission line will usually ensure the integrity of the signal and prevent problems, even without far-end termination.

*always 5 part ~*

# Driving Multiple Lines



LMH6723/4/5 (100 mA Output)

LMH6672 (500 mA Output)

$$R_{EQ} = \frac{R_S + R_L}{N}$$

$$R_S = Z_0 - N R_{DR}$$

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When driving multiple transmission lines, the load presented to the amplifier (or driver) is  $R_{EQ}$ , above, where (assuming all transmission lines have the same impedance):

$R_{EQ}$  = equivalent load seen by the line driver       $R_S$  = source terminating resistance

$R_L$  = load terminating resistance       $N$  = number of transmission lines

The LMH6723, LMH6724, and LMH6725 amplifiers suggested here are single, dual, and quad devices capable of 100 mA output per driver and consume just 1 mA of supply current per amplifier. The LMH6672 is a single amplifier with 500 mA output capability and consumes about 7 mA of supply current.

Do not ignore the output impedance of the amplifier/driver, even though this impedance is usually very low. Even in a closed-loop configuration, the output impedance of the amplifier may be significant at high frequencies. The value of the source resistor should follow this equation:

$$R_S = Z_0 - N \times R_{DR}$$

$R_S$  = source termination resistor value       $Z_0$  = characteristic line impedance

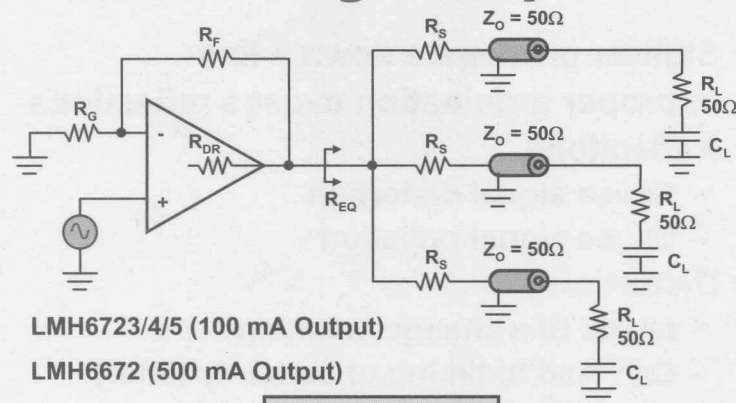
$R_{DR}$  = effective output resistance of line driver at frequency       $N$  = number of driven lines

Without this consideration, any reflections on one transmission line will effect what is happening on the other lines. That is, if the load termination resistors are not optimum, the reflections back to the line driver from one line may couple into the other lines. If the timing of the reflections are different, signal integrity could be compromised.

The problem here might be in the dividing of the signal. This can be compensated for by increasing the gain of the amplifier. This may not be so easy, however, if the source has a fixed amplitude, as in the case of a crystal-based oscillator.



# Preserving DC Signal Average When Driving Multiple Lines



$$C_L \geq \frac{4 \times t_{PR} \times L}{Z_O}$$

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Adding a capacitor in series with the terminating resistor will preserve the average (DC) component of the signal. The minimum value of this capacitor is as indicated here. The problem with this is that the capacitor will slow the rise and fall times of digital signals, effectively delaying the signal.

In the formula above,

$C_L$  is the capacitor in series with the load resistor.

$t_{PR}$  is the signal propagation rate down the board

(about 150 pS/inch, or 60 pS/cm with FR-4 board material).

$L$  is the line length in units consistent with those of  $t_{PR}$ .

$Z_O$  is the characteristic impedance of the line.

Of course, the lines must be controlled impedance ones. The load termination, whether just the resistor,  $R_L$ , or the series  $R_L C_L$ , should be placed near the pin that is driven, but beyond that pin as seen from the clock source.

## ***Signal Integrity***

- **Signals propagate down a line**
- **Improper termination causes reflections**
- **Reflections**
  - Cause signal distortion
  - Cause signal radiation
- **Distortion**
  - Leads to a change in timing
  - Can lead to timing uncertainty (jitter)
  - Jitter causes ADC output noise



8-6



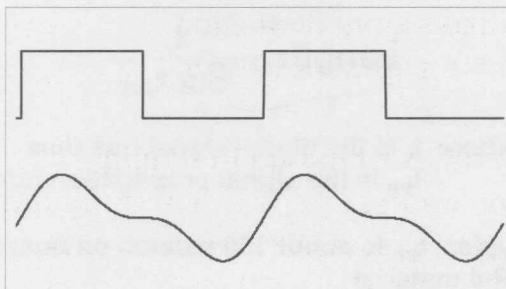
As digital rise times get faster, it becomes necessary to use high frequency analog techniques in the design of printed circuit boards.

All lines carrying signals, digital or analog, are transmission lines, not just simple traces. We can often consider these lines to be simple traces and get away with it, but that can sometimes be a dangerous consideration as far as the integrity of the signal is concerned.

Transmission lines, of course, need to be properly terminated to avoid signal reflections that can cause both distortion and radiation. The distortion, of course, can lead to a change of timing and to jitter. The jitter, in turn, results in noise in the ADC conversion result.

## Reflections

- Signals propagate down a line
- Improper termination causes reflections and signal distortion



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An improperly terminated signal line may distort that signal to the point that it does not go through a device input threshold rapidly enough, resulting in uncertainty in the effective edge timing and in the interpretation as to whether it is a logic high or a low. For clock signals, this can result in misclocking. For an ADC clock, the result can be as mild as a noisy conversion or as serious as a complete malfunction. The nature of the distorted signal will depend upon the degree of impedance mismatch, the number and nature of impedance mismatches along the line, the length of the line, and the propagation rate of the signal across the board.

## When is Termination Needed?

- Simple traces need not be terminated
- Transmission-lines should be terminated
- Trace must be treated as a transmission-line at:

*based on experience*

$$\text{Length} \geq \frac{t_r}{6 \times t_{PR}}$$

Where  $t_r$  is the digital signal rise time  
 $t_{PR}$  is the signal propagation rate

Typical  $t_{PR}$  is about 150 ps/inch on board of  
FR-4 material



8-8



Sometimes we can “get away” with treating a signal line as a simple trace. When **must** a trace be considered a transmission line? The formula here tells us that the line length beyond which a trace **must** be treated as a transmission line is a function of the digital signal rise time and the propagation rate across the board. Nevertheless, it is always best to treat the line as a transmission line.

For analog signals, the rise time is approximated by treating the signal as if it were a trapezoid with edge rates equal to the maximum slew rate of the signal. For monotonic sine waves, the rise time is about 30% of the sine wave period.

# Termination Techniques

- Two Types of Termination

- Series – matches driver output to line

- $R_{\text{source}} + R_{\text{series}} = Z_0$

- AC – matches receiving end to line

- Series RC to ground



8-9



There are two types of termination techniques. Series termination requires that a resistor be added in series with the line close to the signal source. The sum of the source resistance plus the added series resistor should equal to the characteristic impedance of the line. This usually satisfies the termination requirements. Of course, the assumption is that the driven line is a controlled impedance line.

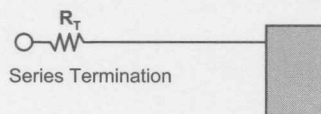
AC termination may be called for when series termination is inadequate because of using the single source to drive many loads, improper termination-resistor value, and/or a non-constant impedance of the line.

Causes of a non-constant line impedance include the use of feedthroughs on the line or having other nearby lines with a non-constant distance from the line under question.

## Series Termination

- **Series termination: a series resistor**
  - Source impedance + resistor =  $Z_0$
  - Resistor placed close to the source
- **Terminate when source to resistor distance :**

$$\text{Length} \geq \frac{t_r}{6 \times t_{PR}}$$



NOTE: See National Semiconductor's Application Note AN-1113 (<http://www.national.com/an/AN/AN-1113.pdf>) for controlling line impedance.



8-10



The driver output impedance plus the external series resistance should be equal to the characteristic impedance of the transmission line. The distance from the source to this resistor is limited by the same equation limiting the length of a simple trace. That equation is repeated here.

Implied here is the fact that the impedance of the line must be equal at all points. The further implication is that stripline- or microstrip-control techniques should be used. The units or  $t_r$  and  $t_{PR}$  must be consistent with each other. For more information, see National Semiconductor Application Note AN-1113.

## AC Termination

- AC termination: series RC to ground at destination

- $R = Z_0$

- C: 
$$C \geq \frac{4 \times t_{PR} \times L}{Z_0}$$

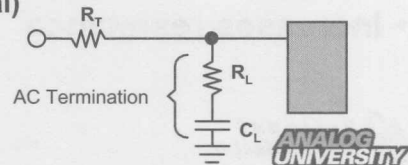
Where  $L$  is the line length

$Z_0$  is the characteristic impedance of the line

$t_{PR}$  is the signal propagation rate down a board trace (about 150 ps/inch with FR-4 board material)



8-11



AC termination consists of a series RC from the line to ground, located near the destination pin but past it as seen from the signal source. The resistor value should be equal to the characteristic impedance of the line and the capacitor value is as indicated here. The units of  $t_{PR}$  and  $L$  must be consistent with each other.

## ***The Skin Effect***

- **Current seeks the path of least impedance**
  - Entire conductor at d.c.
  - Very thin skin above a few MHz
- **Inductance causes current to flow on skin**
- **Reduces conductor cross sectional area**
- **Increases resistance**



8-12



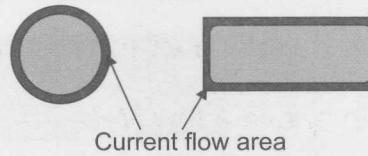
We have learned that current seeks the path of least resistance. The truth is that current seeks the path of least impedance. At DC they are the same, but circuit impedance can be quite a bit higher than circuit resistance at high frequencies. To make matters worse, AC resistance is higher than DC resistance.

Since we are so accustomed to dealing with frequencies in the tens of megahertz, we tend to regard "high" frequencies as something higher than perhaps a few hundred megahertz or a gigahertz. The fact remains, however, that high frequencies, as far as circuit impedances are concerned, are those frequencies beyond just a few megahertz.

DC current flow fills the entire volume of a conductor, but AC current flow is restricted to the surface of a conductor because of the inductance of that conductor. This results in a lower effective conductor cross-sectional area and increased AC resistance.



# The Skin Effect: Skin Current



$$\text{Skin Depth} = \frac{2.6 * K}{\sqrt{f}} \text{ inches}$$

$$K = \frac{1}{\mu_r} \cdot \sqrt{\frac{\rho}{\rho_{cu}}}$$



8-13



The skin effect is caused by the fact that the inductance in the center of a conductor is higher than it is on its surface. This results directly from the fact that the magnetic force radiates from the center of a conductor. The first "line of force" cuts through the entire conductor, but the very last line barely starts out from the center of the conductor before it collapses. It never gets to the surface of the conductor. So, the surface of the conductor has fewer lines of force cutting it and less inductance than the center of the conductor.

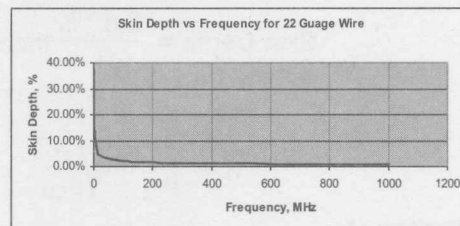
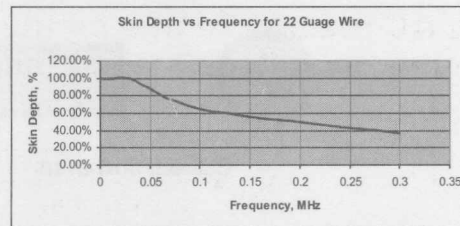
The result is that high-frequency current flows almost exclusively on the surface of a conductor, reducing the effective cross-section area of the conductor and increasing the conductor AC resistance. The conductor may as well be hollow as far as AC current flow is concerned.

The average depth of current penetration, that is, the skin depth, is very shallow and very high frequencies. The distribution of currents in a conductor experiencing the skin effect falls off exponentially as we approach the center of the conductor. The skin depth is as defined here, where  $\mu_r$  is the magnetic permeability of the conductor relative to copper (so is 1 when the material is copper),  $\rho$  is the resistivity of the conductor, and  $\rho_{cu}$  is the resistivity of copper. For copper,  $\rho/\rho_{cu} = 1$  and  $k$  becomes unity.

The next slide shows a plot of skin depth as a percent of wire radius for 22-gauge wire.

# Skin Depth vs Frequency

Freq (MHz)	Skin Depth, %
0.0003	100.00%
0.001	100.00%
0.003	100.00%
0.01	100.00%
0.03	100.00%
0.1	64.74%
0.3	37.38%
1	20.47%
3	11.82%
10	6.47%
30	3.74%
100	2.05%
300	1.18%
1000	0.65%



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The skin effect begins to take effect at about 42 kHz for 22-gauge wire and skin depth falls off rather drastically as frequency increases. These plots show skin depth as a percentage of conductor radius. The lower plot goes from DC to 1 GHz. The upper plot shows detail only out to 300 kHz.

## ***The Skin Effect: AC Resistance***

**The AC resistance of a conductor is much higher than its DC resistance**

$$R_{AC} = \frac{2.61 \times 10^{-7} \sqrt{f \times \rho_r}}{2 \times (w + h)}$$

where  $R_{AC}$  = AC resistance, Ohms/inch  
f = frequency, Hz  
 $\rho_r$  = conductor relative resistivity, compared to copper = 1.00  
w = flat trace width in inches  
h = flat trace height or thickness in inches



8-15

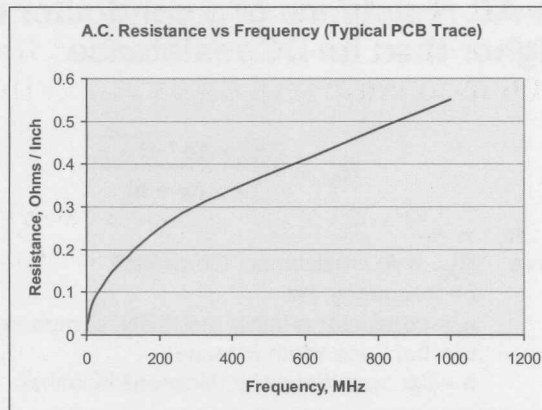


The formula here is for a flat conductor of width "w" and thickness "h".

The rapid falloff of skin depth with frequency tells us that the AC resistance increases rapidly at high frequencies. The AC resistance of a conductor at high frequencies is much higher than its DC resistance. The graph on the next slide illustrates this.

## AC Resistance vs Frequency

PCB Trace 0.006" wide by 0.0015" high	
Freq, MHz	Rac
0.3	0.0095304
1	0.0174
3	0.0301377
10	0.0550236
30	0.0953037
100	0.174
300	0.3013768
1000	0.5502363



8-16



As we see here, the skin effect really does have a big impact upon current flow. This is for a typical one ounce copper trace 6 mils wide.

## AC Resistance

What is the AC resistance in Ohms per inch at 80 MHz of a typical copper PCB trace that is 0.006 inch wide and 0.0015 inch thick?

$$R_{AC} = \frac{2.61 \times 10^{-7} \sqrt{f \times \rho_r}}{2 \times (w + h)} = \frac{2.61 \times 10^{-7} \sqrt{80 \times 10^6 \times 1}}{2 \times (0.006 + 0.0015)}$$

$$R_{AC} = \frac{2.61 \times 10^{-7} \sqrt{80 \times 10^6 \times 1}}{0.015} = \frac{0.00233}{0.015} = \underline{0.1556 \text{ Ohms/inch}}$$



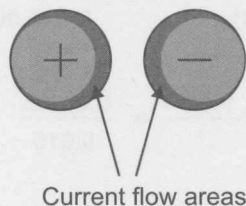
8-17



Let's take a look at the AC resistance of a typical copper trace on a printed circuit board at 80 MHz. Since the trace is a copper one,  $\rho/\rho_{cu}$  is unity. Substituting the frequency and trace dimensions in the equation reveals a resistance that is a real eye-opener. Note this is Ohms/inch!

## ***Proximity Effect***

**The proximity effect on two conductors carrying opposite high frequency currents causes the AC current flow in those nearby conductors to be primarily on the side of the conductors nearest each other**



Current flow areas

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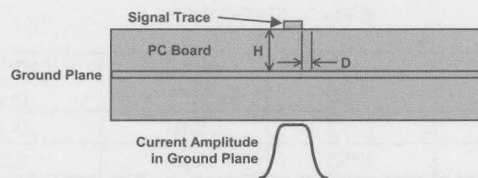
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As conductors come closer together, and/or as frequency increases, the current flowing through two adjacent conductors try to come closer to each other.

DC return currents will fill the entire conductor, where AC currents do not. The path of least impedance is the path where the magnetic fields around the outgoing and return currents are intimately bound together, causing these currents to flow very close together.

In the case of a PCB, this causes ground plane currents to be pretty much confined to a path directly below the corresponding outgoing currents, as though the ground plane was really a return trace immediately below the outgoing line trace.

## Proximity Effect on a PCB



$$I_{RP} = \frac{i}{H \times \pi \times (1 + (D/H)^2)} \text{ Amps/in}$$

where  $I_{RP}$  is the reference plane current density at horizontal distance "D" from the outgoing signal trace

$i$  is the signal current

$H$  is the height of the signal trace above the reference plane

$D$  is the horizontal distance from the edge of the trace.



8-19



The return current in the ground plane follows the outgoing current in the trace above (or below) it rather closely. The current at distance "D" from the edge of the trace falls to less than 4% of the current below the trace when the D/H ratio is 5 and to less than 1% of the current below the trace when the D/H ratio is 10. The result is a current density in the ground plane that is fairly well confined to the area below that current's corresponding outgoing current path.

The current-density formula will tell us the current density at any point in the plane relative to the edge of the outgoing trace, or dimension "D".

Typical dimension "H" will depend upon which layers the trace and plane are located:

- Between an outside layer and an inside layer "H" is typically 75 mills for 4-layer and 6-layer boards.
- Between inside layers "H" is typically 39 mills for 4-layer board or 14 mills for 6-layer boards.

## Ground Resistance

ADC Resolution (Bits)	ADC LSB Size (uV)	ADC Noise (LSB/Inch)	ADC Noise for 3 Inch Trace Length (LSB)
8	7813	0.07	0.2
10	1953	0.28	0.8
12	488	1.13	3.4
14	122	4.51	13.5
16	31	7.74	53.2

Ground plane resistance of 0.055 Ohms per inch (at 40 MHz) with an ADC reference voltage of 2.0 Volts can result in significant ground noise that can affect apparent ADC performance with as little as 10 mA<sub>P-P</sub> of 40 MHz ground current



8-20



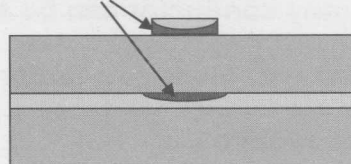
Here we see how 40 MHz noise in the ground plane can be significant. Note that, assuming 0.055 Ohms per inch of ground path resistance, a three inch trace can produce enough ground noise to seriously affect high-resolution ADCs. There is not much effect at 8 bits, but we can begin to see the effect at 10 bits. The noise can be prohibitive at 14 bits and higher. On top of this, the inductance of the path is even higher!

You start to wonder if it is even possible to realize the full noise potential of a high-speed, high-resolution ADC.



## ***Skin Effect + Proximity Effect***

Current flows in a small area of the trace and reference plane.



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The skin effect and the proximity effect combine to limit the current carrying area of the conductor to a very small part of the conductor's cross sectional area. The areas of current flow are actually much smaller than shown here.

# ***Radiation***

- **Any conductor can**
  - Radiate
  - Pick up signals
- **Therefore, any conductor can be an antenna**
- **Greater loop area leads to a better antenna**
- **A plane can radiate**
- **Copper with one point grounded can radiate**



8-22



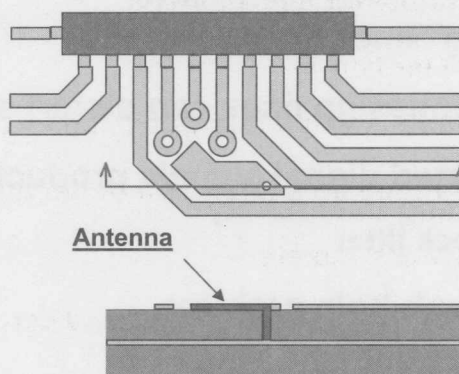
As if the skin effect and the proximity effect were not enough, high-frequency circuits carry yet another problem in the form of EMI. The problem is two-edged: signal radiation and signal pickup.

Governments of virtually all modern nations regulate the amount of interfering energy that can be radiated. This is good because it means there is less energy to be picked up by our circuits. However, we still must guard against our circuits radiating energy at unauthorized frequencies, and good design practice also says we should design our circuits to resist pickup of interfering signals. After all, you never know when a circuit may be exposed to a high field environment.

When outgoing and return currents flow, there is a "loop area" that is defined by the area between the conductors. The larger this area is, the larger is the electromagnetic field "fringing" around the conductors. EM fringing is the cause of radiation, so larger loop areas will radiate and/or pick up more energy than will smaller loop areas. Since high-frequency current flows in a restricted area of a ground plane, the path acts pretty much as a trace and can radiate. This is especially true when the current path through the ground plane is forced to deviate from the outgoing current, as in the case with a split ground plane.

We tend to cover open areas on printed circuit boards with grounded copper. However, if we ground that copper area at a single point, we could create an antenna.

## Built-in Antenna



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The rationale behind covering open areas with grounded copper is to get as much area as possible between ground plane and power plane. This will provide a high power-plane-to-ground-plane capacitance that is much more effective than a physical capacitor. We do this because of the non-ideality of physical capacitors.

However, areas of copper that are grounded at only one point, as seen here, act as monopole or “whip” antennas.

Here we see a cross-section of the printed circuit board as seen from the edge of the board if we cut it at the arrowed line. The antenna is readily identified.

Any signal current that flows through the point in the ground plane where this grounded area is connected, and is within the bandwidth of that antenna, is radiated by that antenna. Of course, the antenna is rather small, so it may be harmonics of the ground-plane energy that are radiated.

These antennas also can pick up electromagnetic field energy and feed that energy into the ground plane. Unless the field is very strong, however, there may not be enough energy to have a detrimental effect. Of course, you never know if your circuit might be subjected to a high field-strength environment.

Using copper areas that are ungrounded altogether is also bad because not only do these isolated conductors serve no useful purpose, but they can act also as “directors” to focus and enhance signal energy or as “reflectors” to reflect signal energy back to a main antenna element, which may be another signal line.

In summary, floating copper areas should be eliminated or grounded at multiple points. Grounded copper areas should be connected to ground at rather close intervals, generally no more than about 1-inch spacing, forming a grid on the grounded surface.

## ***Signal Traces vs. Transmission Line***

- “Long” lines are not traces
- Transmission lines can distort signals
- Distorted digital signals produce:
  - Timing uncertainty
  - Clock jitter
- Through-hole problem
- Layout can be critical



8-24



Here is a brief review of some important points we have covered.

All signal-carrying lines are transmission lines. Beyond a certain length we absolutely must treat them as such if we are to avoid signal distortion, timing problems and jitter.

Through-holes in a transmission line create impedance discontinuities and cause reflections with their attendant distortion and noise problems. A through hole in a PCB has about 1 to 1½ nanoHenries of inductance, which can create problems. For example, a 14-bit, 80 MSPS ADC must have bypass capacitors that are no more than 2 to 3 millimeters from the bypassed pins. Putting these capacitors on the opposite side of the board results in the capacitors being isolated from the ADC by the ¼ to ¾ Ohm (at 80 MHz) of the through-hole inductance plus another ¼ Ohm or so in the trace inductance.

Layout is critical for transmission lines as these can experience impedance discontinuities when other lines approach them and depart from them. This is true even of the return current paths in the ground plane.

*Vias are  
inductors.*

## ***Maximum Trace Length***

**All traces are transmission lines, but a trace length longer than this absolutely must be treated as a transmission line:**

$$L_{MAX} = \frac{t_R}{6 \times t_{PD}}$$

where  $L_{MAX}$  is the maximum line length beyond which that line must be considered a transmission line

$t_R$  is the signal rise time

$t_{PD}$  is the signal propagation rate down the board

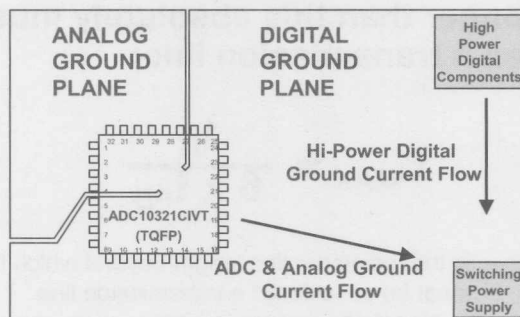


8-25



We have shown that a PCB trace can become a transmission line at a surprisingly short distance. Digital rise time (NOT repetition rate or frequency) is what we use to determine maximum trace length before it must be considered a transmission line. For analog signals, we can use 30% of the period of the highest frequency component, divided by its peak-to-peak amplitude, in the signal in place of rise time.

## Previous Suggestion



8-26

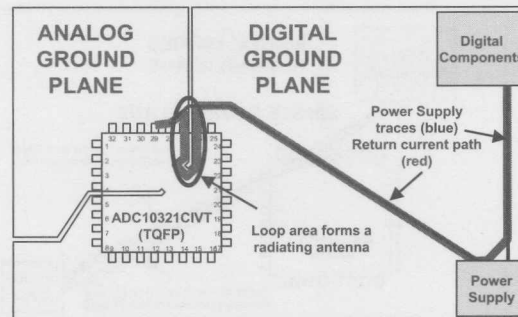


We already alluded to the fact that the split ground plane can lead to problems when lines carrying signal currents cross the split between the planes. Of course, analog components will be kept in the analog area of the board and digital components in the digital area. This keeps analog and digital return currents away from each other. We have already seen that high frequency or high-edge rate signals see a high resistance, even in a ground plane, so we know the need to keep analog and digital return currents separated from each other.

The layout shown here is one that we previously advocated and makes an attempt to isolate analog and digital ground currents, but ignores EMI effects. We have also found that this method works well up to 50 MSPS for 10-bit ADCs and to about 30 to 35 MSPS for 12-bit ADCs. Beyond that we see excessive circuit noise. The split ground plane can also lead to signal radiation, as we will see.

The ADC10321 is a 10-bit, 20 MSPS ADC.

## Loop Area Will Radiate



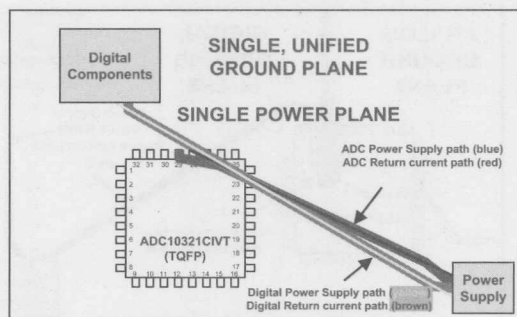
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8-27

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Here is a board with a split ground plane, as we have previously advocated. It can be effective in limiting the path of ground currents to desired areas and minimizing ADC noise. However, when we use supply traces to control the analog and digital power paths, we see that the return ADC current must deviate from the the outgoing current path. This produces a current loop that can radiate.

# Single Ground Plane and a Power Plane



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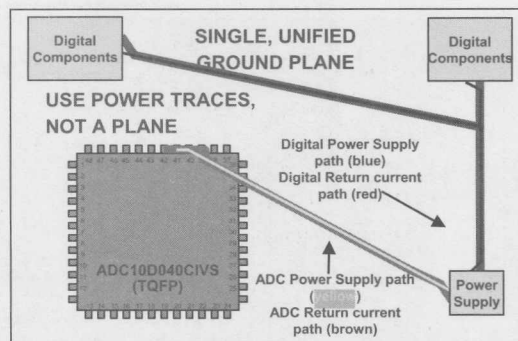
8-28

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We can eliminate the loop-area problem and minimize the radiation problem by using both a ground plane and a power plane. This allows the outgoing and return currents to flow close to each other and minimize RFI/EMI problems. The problem now, however, is that component placement relative to other components is very important as common analog and digital return current paths can lead to digital noise in analog circuits.



# Single Ground Plane, Power Traces, Careful Routing



8-29



If we remember that the proximity effect causes outgoing and return currents to flow as close to each other as they can, we realize that we can control the path of return currents in the ground plane by careful component placement and thoughtful routing of all traces, including those of the power supply. Ground return currents will follow their respective outgoing traces and thus we can keep analog and digital return currents away from each other.

The single ground plane eliminates loop areas and the signal and power traces control current flow, even in the ground plane.

Analog and digital components should be located in their own, dedicated areas of the PC board. The power supply should be located at a board edge or corner and between analog and digital areas. Layout of power supplies can be critical for noise performance, but that is beyond the scope of this presentation.

Digital components (especially high-speed, high-powered digital components) must not be placed on or near the path that analog return currents follow in getting back to the power supply. That is, they should not be located near lines carrying analog currents or power supply lines to analog or mixed-signal components.

Remember that power supply lines carry signal currents because they recharge bypass capacitors on the board. Their return currents must go through the common junction of a split ground plane, flowing away from the outgoing (power) trace/path. This forms a loop area that will radiate. Sometimes this radiation can be picked by low-level analog circuits.

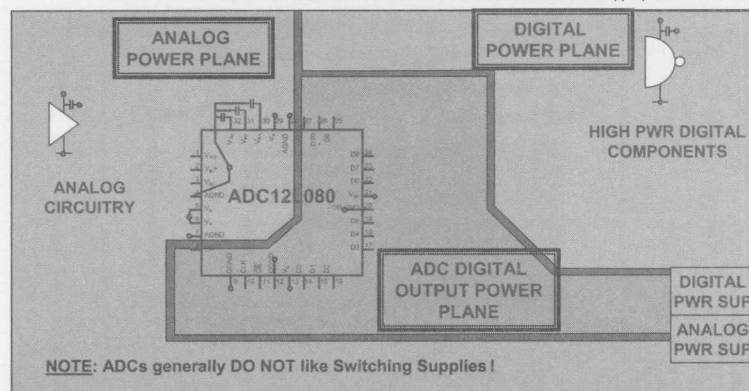
The main problem with this method is the high impedance of the power distribution system, leading to difficulty in proper power supply bypassing.

The ADC10D040 is a dual 10-bit, 40 MSPS ADC with either single or dual output bus capabilities. A 20 MSPS version is available in the ADC10D020.

# Recommended ADC Layout Example

## Use a Single, Solid Ground Plane

• Green dots are vias to appropriate PWR or GND plane



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This recommended ADC layout will allow the best performance the ADC can offer. To summarize the requirements:

Use a solid, unified ground plane. DO NOT split the ground plane. If there are ground planes in more than one board layer, connect them all together with a grid of through holes (vias) on a spacing of one inch or less.

Split the power plane, keeping each power plane in the same board layer. There should be separate power planes for (1) analog circuitry, (2) digital circuitry, and (3) the ADC digital-output drivers.

Use analog power for the digital core supply, but NOT for the digital-output drivers.

The power for the ADC digital-output drivers may be the same supply as for the component(s) driven by the ADC outputs.

Locate all analog components and lines over the analog power plane and all digital components and lines over the digital power plane.

If any digital circuitry is powered by the same supply as the ADC output drivers, and has signals lines going to the other digital area of the board, use capacitors between the two power planes. Locate these capacitors very close to the signal lines.

Use separate power sources for each plane. The ADC digital-output power can come from either power source, but should be decoupled with a series choke.

The ADC12L080 is a low-power 12-bit, 80 MSPS ADC intended for wireless communication applications.

## ***Summary of Layout Rules***

- **Use A Single, Unified Ground Plane**
- **Split Power Planes**
- **Let Trace Routing Control Ground Currents**
- **Tie Down Grounded Copper Areas at Many Points**
- **Remember: Traces Are Transmission Lines**



8-31



Here is a summary of rules for maximizing ADC and mixed-signal performance. While originally intended as guidelines for high-speed circuits, we find that these guidelines are equally applicable to lower-speed circuits because of the fast digital edge rates we have today. It is these edge rates, not frequency, that determine circuit and layout needs.

All signal carrying lines are transmission lines. Beyond a certain length, we absolutely must treat them as such if we are to avoid signal distortion, timing problems, and jitter.

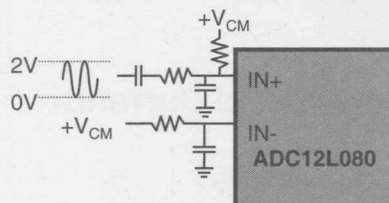
Through holes in a transmission line create impedance discontinuities and cause reflections with the distortion and noise problems that come with reflections. A through hole in a PCB has about 1 to 1½ nano-henries of inductance, which can create problems. For example, a 14-bit, 80 MSPS ADC must have bypass capacitors that are no more than 2 to 3 millimeters from the bypassed pins. Putting these capacitors on the opposite side of the board results in the capacitors being isolated from the ADC by the ¼ to ¾ Ohm (at 80 MHz) of the through-hole inductance plus another ¼ Ohm or so in the trace inductance.

Layout is critical for transmission lines since they can experience impedance discontinuities when other lines approach them and/or depart from them. This is also true of the return current paths in the ground plane.

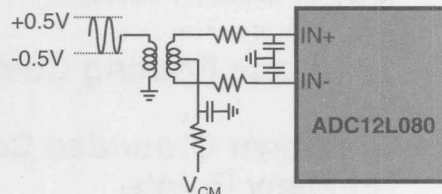
Much of this takes us back to what some of us learned in school but never used.

# Single-Ended Input to Differential - Input ADC

NOT Preferred Way



Best Way



**NOTE:** Performance with a single-ended input signal is not as good as with a differential-input signal! This is true of ALL differential-input ADCs.



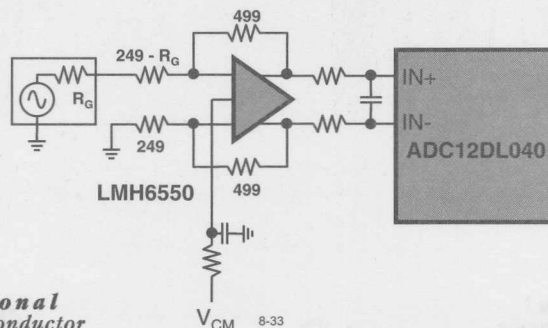
8-32



The method of using differential-input ADCs to convert single-ended signals will determine the performance of the circuit. Biasing one input and driving the other input will work, but distortion performance is compromised. Using a transformer to convert the single-ended signal to a differential one works very well and is the preferred method.

# Single-Ended Input to Differential Input for DC and Low Frequencies

The best single-ended to differential solution for AC and low-frequency applications is to use a fully differential amplifier



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Sometimes, however, the requirements include very low frequency or DC inputs to the ADC such that a transformer cannot be used. In such cases a fully differential amplifier, such as the LMH6550, will provide an excellent solution.

The ADC12DL040 is a dual 12-bit, 40 MSPS low power ADC offering high performance (11.1 ENOB) while consuming just 210 mW.



8-34





## ***A/D Conversion Products and Application Examples***

1

While this seminar has focused mainly on the successful use of ADCs, what follows is a brief summary of the characteristics of the some of our ADC product types and some specific applications.



# ***National's Data Converters***



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ADCs, DACs  
High Speed Family  
General Purpose Family

### **Leading supplier in Many Applications**

Communications  
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Digital TV  
Instrumentation  
Imaging  
Portable Systems  
Control Systems  
Etc.

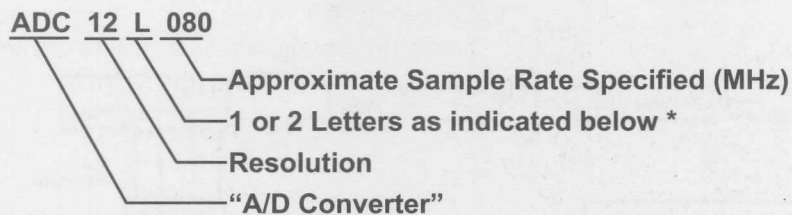
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9-2

We take pride in the high performance at the lowest power of our data converter products. Our product offerings are in resolutions between 8 and 14 bits, with the majority of them in the 8 to 12 bit area. Application space includes virtually all commercial areas.



## ***Part Numbering Convention for High Speed ADCs***



- \* D – Dual
- T – Triple
- Q – Quad
- L – Low Voltage (3.3V or less)
- B – FIFO Buffer
- S – Serial (LVDS/SLVS) Outputs



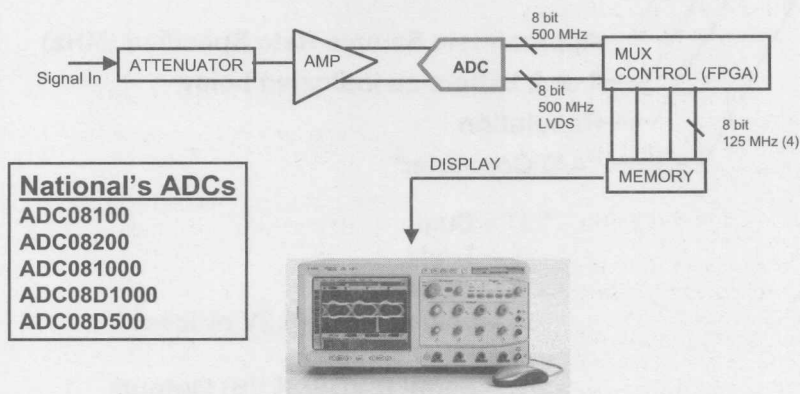
9-3



While there are some exceptions to this method of specifying our products, this method generally holds for newer devices. The letters following the resolution may be combined, as in the cases of the ADC12DL066, which is a dual, low voltage, 12-bit, 66 MSPS ADC.

At this time we do not have any quads or triples being offered, but they are planned.

## Example Application: Digital Oscilloscope



9-4



This digital oscilloscope block diagram is an example of an application for the ADC08D1000 and other very high speed converters. Other applications for this excellent high speed ADC include, but are not limited to:

- Direct RF Down Conversion
- Satellite Set-Top Boxes
- Communications Systems
- Test Instrumentation
- Data Acquisition

The ADC08D1000 is the best choice anywhere a high input bandwidth (up to 1.7GHz), very fast sampling frequency (up to 2.6GSPS) ADC with low power consumption, temperature stability, linear phase response, and low BER performance are required.

# **ADC08D1000**

## **Dual 8-bit 1GSPS ADC**

### **Features**

- Single 1.9V Power Supply
- Output data rate
  - 1:2 demux: 2 output channels interleaved to provide 500MSPS/channel (LVDS)
- Differential inputs
- Internal voltage reference
- Buffered Internal sample and hold
- Dual Edge Sampling (interleaving)
- Double Data Rate support
- Synchronization between multiple channels
- Full-scale (gain) and offset adjustment of each ADC (I & Q).
- 128-pin EP LQFP package



### **Key Performance Metrics**

- Resolution: 8 bits
- Conversion rate: 1GSPS

#### **Specifications @ $F_{in} = 500\text{MHz}$**

- ENOB 7.4 bits
- DNL  $\pm 0.15$  LSB
- INL  $\pm 0.30$  LSB
- SNR 47.1 dB
- SFDR 55 dB
- SINAD 46.3 dB
- THD -55 dB
- Power consumption
  - Normal Operation: 1.6W (typ)
  - Power Down Mode: 20mW (typ)



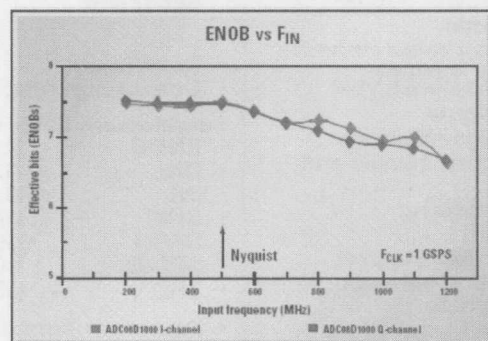
9-5

The ADC08D1000 is a dual 1GSPS ADC with input channels labeled I & Q.

Both converters on the die have fully differential inputs with a maximum input signal range of 950mVp-p. Each converter has a 1:2 demultiplexer that feeds two LVDS buses and reduces the output data rate on each bus to half the sampling rate. A choice of SDR and DDR is available and an output data clock eases data capture.

The two converters may be interleaved such that they both sample the input signal at the user's choice of either input. In this Dual Edge Sampling (DES) mode, the two converters sample the one signal on opposite edges of the ADC input clock, so that the net sample rate is twice the input clock frequency. This provides an overall sample rate that is twice the ADC clock rate. Since the ADC08D1000 is specified for 1 GSPS, the overall sample rate in the DES mode is guaranteed at 2 GSPS. Since the ADC08D1000 will typically perform at 1.3 GSPS, the DES mode can provide a 2.6 GSPS conversion rate.

## ADC08D1000 Unparalleled Performance

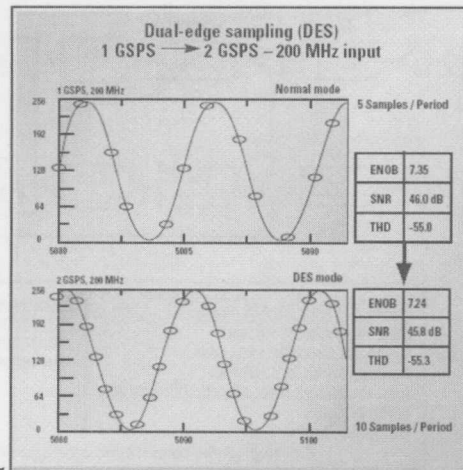


9-6



The ADC08D1000 maintains excellent ENOB over its full input frequency range. This performance is achieved by incorporating trimmed input termination resistors at the analog signal inputs, avoiding the stub problems commonly seen when input termination is done on the printed circuit board.

## Dual-Edge Sampling (Interleaving)



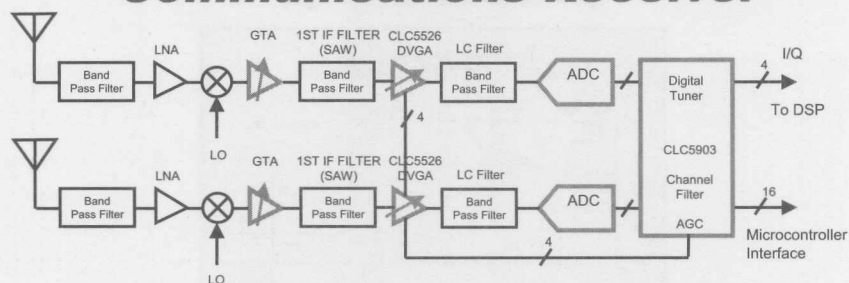
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In DES mode, the performance is still excellent at a sample rate of twice the clock frequency, exceeding the performance of any competitive converter.

## Example Application: Communications Receiver



### National's ADCs

ADC12L066/ADC11L066  
ADC12DL066/ADC11DL066  
ADC12L065/ADC12DL065  
ADC12L080/ADC12L080W/ADC12DL080  
ADC12QS065  
CLC5957

### National's Diversity Chipset:

CLC5903 (GSM projects)  
CLC5526 - DVGA  
CLC5506 - GTA

Coming: A family of 14-bit, high-speed products

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Our high speed products provide superior performance in communication systems, as well as in medical and general instrumentation, RADAR, and other systems requiring high sample rates, including those where undersampling is used.

# **ADC12DL066**

## **Dual 12-bit 66MSPS ADC**

### **Features**

- Wide dynamic range
- IF sampling capability
- Full power bandwidth – 450MHz
- 2Vpp differential input range
- On-chip reference buffer
- Pipeline architecture with digital error correction
- 3.3 V supply
- 64-pin TQFP package



### **Key Specs**

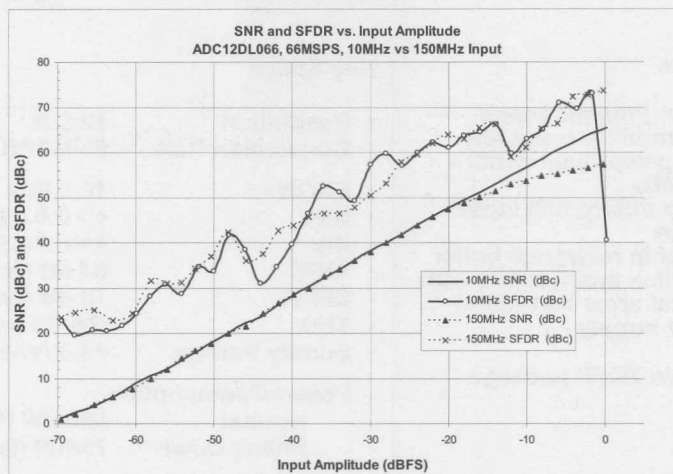
- Resolution 12 bits
- Conversion Rate 66 MSPS (min)
- ENOB 10.5 Bits (typ)
- DNL +/- 0.4 LSB (typ)
- INL +/- 0.7 LSB (typ)
- SNR 64 dB (typ)
- SFDR 78 dB (typ)
- THD -74 dB (typ)
- Supply Voltage +3.3V+/-5%
- Power Consumption
  - Normal 686mW (typ)
  - Power Down 75mW (typ)

9-9



The ADC12DL066 is one of our dual high-speed, 12-bit ADC offerings. As with those other products, the ADC12DL066 offers excellent performance at low power consumption levels, together with a very high (450 MHz) full power bandwidth.

## ADC12DL066: 10MHz & 150MHz Input Amplitude SNR & SFDR



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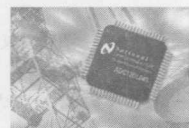
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The excellent performance of the ADC12DL066 over a wide range of input levels, both at 10 MHz and at 150 MHz, can be seen here. Note the near ideal level performance.



# ADC12DL040/65

## Dual 12-bit 40/65MSPS



### Features

- Industry's Lowest power consumption
- Single +3V/3.3V operation
- On chip precision reference
- Straight binary or 2's complement outputs
- Duty cycle stabilizer
- Parallel or Mux'd outputs
- 64 pin TQFP package
- Pin compatible ADCs:
  - ADC12DL066
  - ADC12D040



### Key Specs

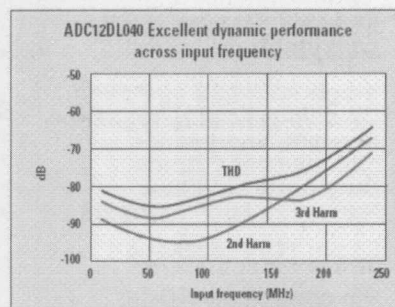
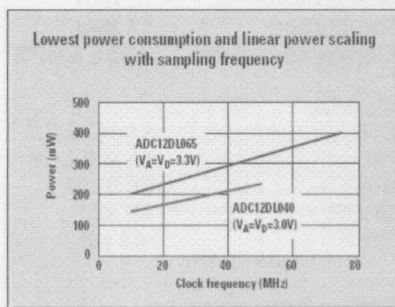
- Resolution 12 bits
- Conversion Rate 40/65 MSPS
- @ Nyquist
  - DNL +/- 0.3 LSB
  - INL +/- 0.8 LSB
  - SNR 68.5 dB
  - SFDR 85 dB
  - THD -83 dB
- Power Consumption
  - Normal 210 / 360 mW
  - Power down 36 mW

9-11



This recently introduced dual ADC offers excellent performance with extremely low power consumption. The 250 MHz full power bandwidth and dual nature of this device, together with its excellent performance, enables efficient, space-, and cost-saving designs of many systems, including communications and instrumentation, among others. A single, 5V, 40 MSPS version (ADC12040) is available and is pin-compatible with our other 12-bit high-speed ADCs.

## **ADC12DL040/65 Performance Charts**



9-12



The low power consumption of the ADC12DL040 and the ADC12DL065 scales in a linear manner with sample rate so that there is no excess power consumption when operating at lower sample rates. Note also the excellent distortion performance, even at very high input frequencies.

## **ADC12L080**

### **12-bit 80 MSPS ADC**

#### **Features**

- Wide dynamic range
- IF sampling capability
- Full power bandwidth – 450MHz
- 2Vpp differential input range
- On-chip reference buffer/external reference
- Pipeline architecture with digital error correction
- Single 3.3 V supply
- 32-pin TQFP package
- Pin compatible with:
  - ADC12010
  - ADC12020
  - ADC12040
  - ADC12L063
  - ADC12L066

#### **Key Specs**

- |                     |             |
|---------------------|-------------|
| • Resolution        | 12 bits     |
| • Conversion Rate   | 80 MSPS     |
| • ENOB              | 10.7 Bits   |
| • DNL               | +/- 0.4 LSB |
| • INL               | +/- 1.2 LSB |
| • SNR               | 66 dB       |
| • SFDR              | 80 dB       |
| • SINAD             | 66 dB       |
| • THD               | -77 dB      |
| • Power Consumption |             |
| – Normal            | 430mW       |
| – Power Down        | 40mW        |



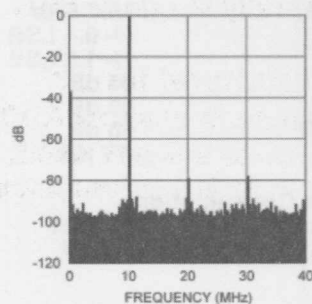
9-13



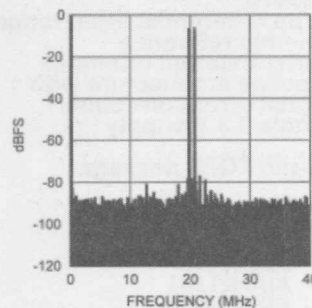
The high-speed, high-bandwidth ADC12L080 is among the latest in our line of high-speed ADCs, pushing toward faster sample rates. Note the pin-compatibility with many of our other high speed ADCs. The next page gives some insight into the performance of this product.

## ***ADC12L080 – Dynamic Performance***

**Spectral Response  
150 MHz Input**



**IMD  
19.6 MHz & 20.5 MHz**

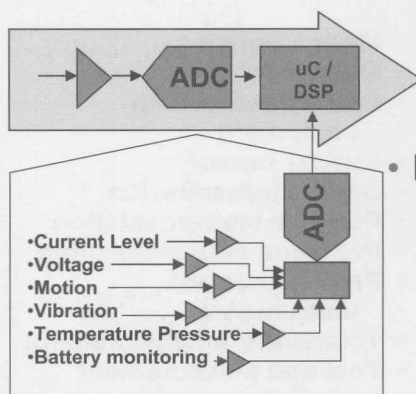


9-14



These plots show the excellent performance of the ADC12L080. Note the excellent distortion and intermodulation performance.

## General Purpose ADCs - Two Application Areas



- **In the Signal Path:**

- Primary measurement and control
- Generally single or dual ADC

- **For Peripheral Input:**

- Often multi-channel ADC
- Measures system health, reliability & performance
- Monitors system environment

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General Purpose ADCs can be found deployed in two key application areas:

The signal path is the most obvious area where the ADC provides the main system interface between a critical real-world signal and the processing block (DSP, uC, ASIC).

But there is also a need for ADCs in system health, reliability, and performance measurement. This is where the majority of general purpose ADC applications are found. This is because these environmental signals do not generally need to be digitized to very high resolution as order of magnitude data used in coarse decision making is sometimes all that is required. These functions often revolve around many system inputs (multiple supply voltages for instance) and can often need many more I/Os than are available on low cost  $\mu$ Cs.

# ***General Purpose ADC Applications***

***General Purpose ADC applications are Everywhere!***

- Battery monitoring
- Battery-powered instruments
- Car Navigation
- Communications
- Current / Voltage monitoring
- Instrumentation and control
- Interface to transducers
- Industrial equipment
- Medical instrumentation
- Mobile communications
- Motion Sensing
- Motor control
- Optical networking equipment
- Optical sensor
- Optical transmission
- Portable instrumentation
- Precision data acquisition
- Process control instruments
- Temperature measurement
- Test and measurement systems



9-16



General purpose ADCs are used across all industries. There are applications in medical, industrial, consumer, automotive, communications, and computer related markets. More than 65% of discrete ADCs sold are of 8-, 10-, and 12-bit resolution.

## ***Application Trends in General Purpose ADCs***



- Need for higher speed, smaller pkgs
- Move from parallel to serial interfaces (SPI, I2C)
- Intelligent partitioning, especially below 90nm



- Analog does not scale like digital
- Supply voltage gets too low
- Analog performance degrades



- System health, reliability and performance monitoring increases.



- Number of integrated ADCs no longer sufficient



9-17



The introduction of this new general purpose ADC family is a major event for National. The big news is that the complete family comprises 36 base parts. With this family introduction we are hitting the market with a broad range of guaranteed components to cover a wide variety of applications.

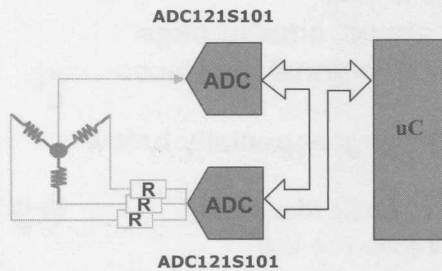
With such a broad selection of parts, we're able to offer customers a simplified approach to component selection. Our family offering is pin compatible for example.

The family also goes a long way to remove any mystery hidden in ADC specs often the case with competing offerings. For instance, these parts are guaranteed from +2.75V to +5.25V, so can be used in a wide variety of systems almost regardless of the supply level. These devices also operate over an extended temperature range and offer equal or better performance than competing solutions with higher linearity and dynamic performance in a low power solution. Our small packaging also contributes to reduction in PCB real-estate.

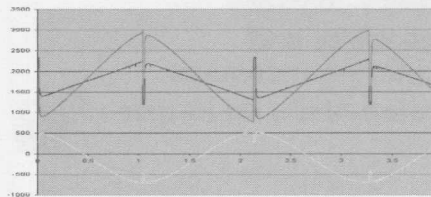
Finally, we've adopted a part numbering scheme we hope will de-mystify our products and make them easier to specify. Our part number scheme allows easy recognition of resolution, input channel options, as well as reference and power supply options. We hope this goes a long way to making our general purpose family the most accessible portfolio on the market and help secure our future success in this important product category. More on this later.



# Third Harmonic Sensorless Brushless DC Motor Monitor



- ADC1- ADC2 is the third harmonic of the motor.
- The commutation should be done on each min/max



- Midpoint
- Recreated Midpoint
- Third Harmonic

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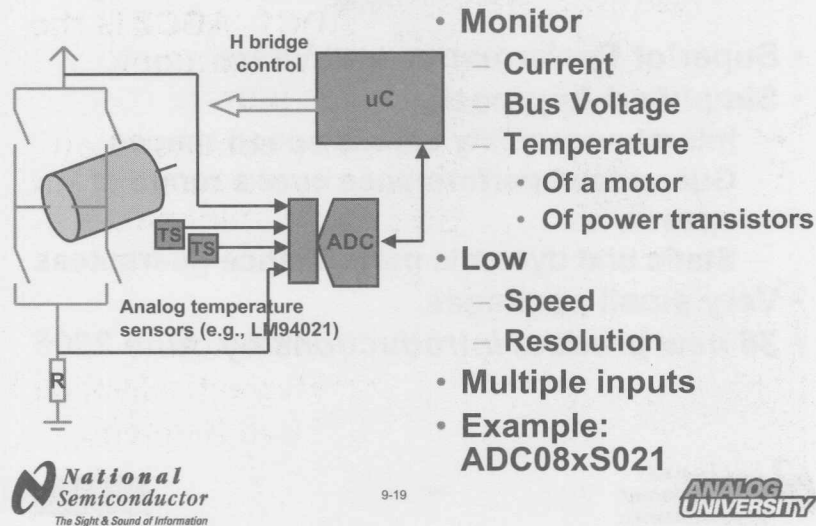
One way to control a Brushless DC motor without hall sensors is to monitor the third harmonic. This method is detailed in IEEE article "Indirect sensing for rotor flux position of permanent magnet ac motors operating over a wide speed range". This method is an alternative to the zero crossing Back EMF method and has numerous benefits such as wider operating speed range, higher precision and high acceleration/deceleration rate acceptance. It can also work with PWM control and without mid point access.

The method is based on the fact that the voltage between the mid point and the recreated mid point (with the 3 resistors) is the third harmonic of the motor. Each minimum or maximum of this signal will represent the commutation time for the switcher.

This solution implements two single ADCs in a simultaneous sampling configuration. It can also be implemented with a differential amplifier when the resistors are perfectly matched, but this might be more expensive than the use of a second ADC.



## General Purpose ADCs are also used for Peripheral Control



One common application is the monitoring of a motor's performance: bus voltage, current drawn, temperature, speed, and vibration. Small ADCs with an input multiplexer can easily fit the small form factor of motor drives.

## ***General Purpose Converter Products***

- **Superior Performance and Value**
- **Simplified Approach**
  - **Interchangeability across speed ranges**
  - **Guaranteed performance over a range of speeds**
  - **Static and dynamic performance guarantees**
- **Very small packages**
- ***36 new product introductions by June 2005***



9-20

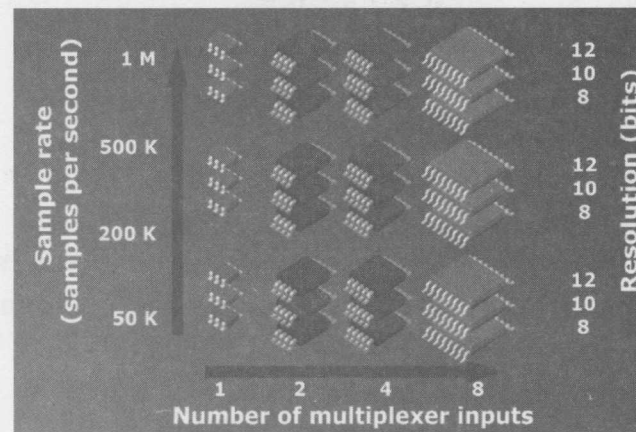


The introduction of this new general purpose ADC family is a major event for National. The big news is that the complete family comprises 36 devices. With this family introduction we are hitting the market with a broad range of guaranteed components to cover a wide variety of applications.

With such a broad selection of products, we are able to offer customers a simplified approach to component selection. Our family offering is pin compatible, for example. The family also goes a long way toward removing any mystery hidden in ADC specs that often shroud competing offerings.

Most of our newer general purpose ADCs are offered with a unique guarantee of performance over a range of clock speeds. Typically, a designer may choose an ADC with a specified sample rate that is close to but not an exact match to the clock rate required by his or her system, realizing that ADCs will generally function adequately a somewhat above and below the application clock rate. This usually presents no problem, but our new general purpose ADCs offer performance guarantees over a range of clock rates, rather than a single rate, so you know expected performance at the exact clock rate needed.

## National's New General Purpose ADC Portfolio



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**More options are coming!**

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All of our newer ADCs of a given number of channels come in the same package with the same pin configuration, making it easy to migrate to different resolutions and speed ranges.

## ***Three Standard Speed Ranges, Three Resolutions***

*National offers Guaranteed Performance  
over a Range of Speeds!*

- **Speed Ranges:**
  - 50ksps to 200ksps
  - 200ksps to 500ksps
  - 500ksps to 1Msps
- **Easy migration across speeds and resolutions from 8-12Bit with only one layout saves cost and time!**
- **Wide supply voltage from +2.7 to +5.25 V**
- **Specified industrial temperature -40°C to +85°C**
- **Some operating temperatures -40°C to +125°C**

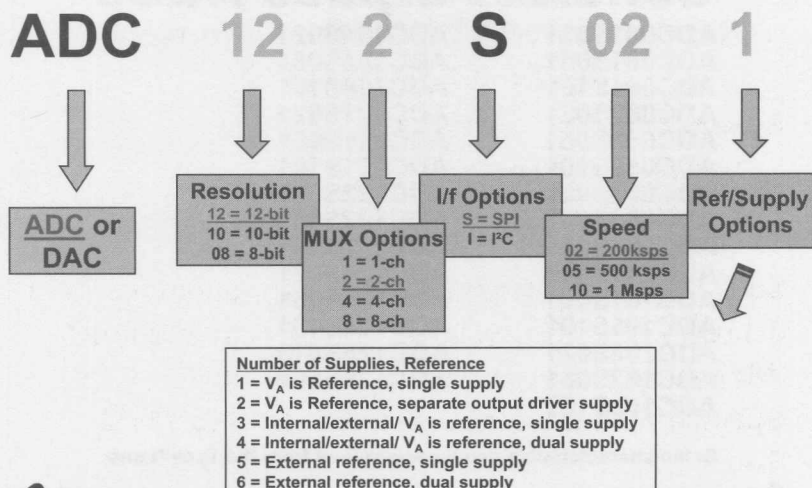


9-22



National's Family ADCs are guaranteed across a range of speeds. This is unique in the industry. Conventional ADCs are guaranteed at only one speed, so it can take 5 or 6 competitive devices to cover the same range of speeds National covers with a single product. Customers who use a variety of conventional general purpose ADCs can standardize on just a few National ADCs.

## Descriptive Part Numbering



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We have developed a new part numbering scheme which we hope will make our products more accessible and easier to specify.

The graphics here show the important aspects of the part number, with the first two numeric digits indicating the resolution of the ADC. The next indicates the number of input channels (multiplexer). The next place indicates the interface. This initial offering concentrates on providing an industry standard SPI interface compatible with a wide range of industrial microcontroller products.

The inset clarifies the three speed grades we offer relative to the three resolutions. However, the last three digits can sometimes seem arbitrary against this stated "standard".

## ***Some of Our New General Purpose ADCs***

ADC081S021	ADC104S021
ADC081S051	ADC104S051
ADC081S101	ADC104S101
ADC082S021	ADC121S021
ADC082S051	ADC121S051
ADC082S101	ADC121S101
ADC084S021	ADC122S021
ADC084S051	ADC122S051
ADC084S101	ADC122S101
ADC101S021	ADC124S021
ADC101S051	ADC124S051
ADC101S101	ADC124S101
ADC102S021	ADC128S013
ADC102S051	ADC128S102
ADC102S101	

Some characteristics can be determined from the Type Name



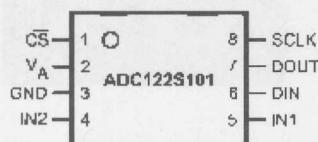
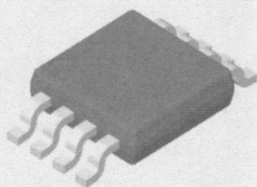
9-24



This partial list of our newer general purpose ADCs. Note that the resolution, number of channels and interface type can be determined from the device type.

## ***Example: ADC122S101***

- 12 bit, 2 channel, SPI interface, 1Msps, Single supply



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- 8 pin MSOP Pkg 3 x 5 mm
- No External components needed
  - V<sub>A</sub> used as reference
  - SPI Clock is used as ADC clock
- Outstanding Performance
  - ENOB: 11.7 bits (typ)
  - DNL: +0.9 / -0.6 LSB (typ)
  - INL: ± 0.64 LSB (typ)
  - 4.3 mW (typ) @ 3V Supply

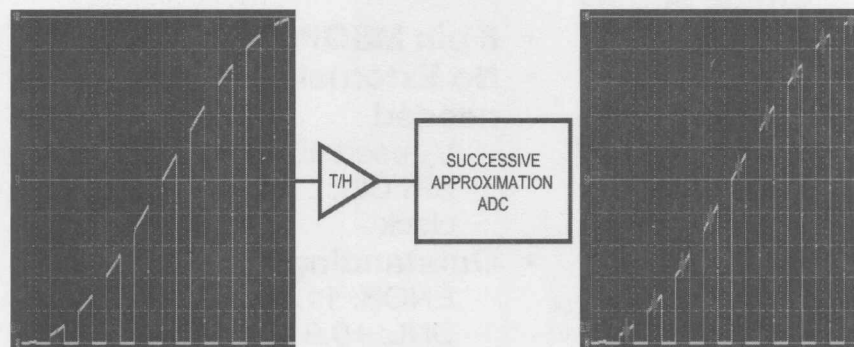
9-25

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Here is an example of our newer products. All of our newer 12-bit offerings have about the same performance indicated here, whether 1, 2, 4 or 8 input channels. Similar products of different resolutions are pin and functionally compatible with each other.



## Wide Input BW Allows Synchronous Sampling(1)



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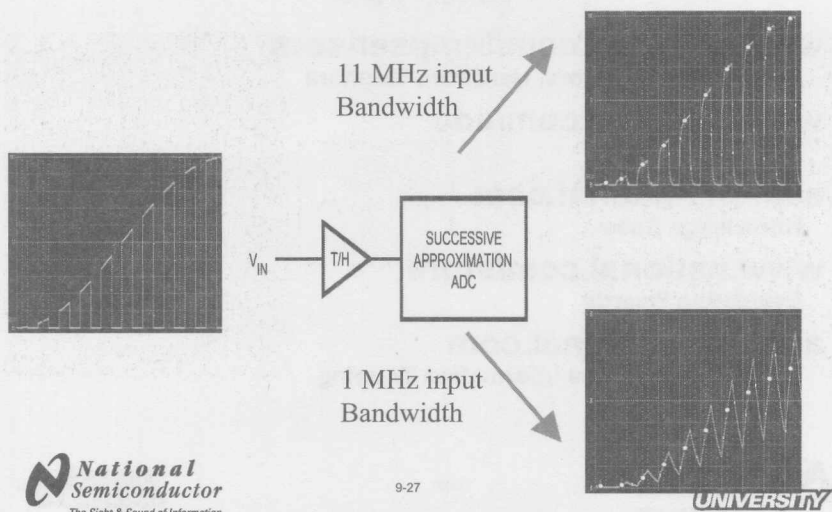
9-26

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We end today's seminar with an application example of a 25 kHz sine wave which is switched at a 500 kHz frequency. A common method of acquiring the original 25 kHz signal is to synchronize the acquisition with the PWM "on" time. The red crosses indicate the sampling points, which will remove the PWM. But what happens if the input bandwidth is not high enough?



## Wide Input BW Allows Synchronous Sampling(2)



If the ADC input bandwidth is not high enough, the the PWM frequency is filtered because of signal slew rate limiting and the measurement is adversely affected.

The left picture is the signal as it exists, while the two pictures on the right indicate what the ADC "sees". With 1 MHz input bandwidth, The ADC sees a different signal than that expected.

## ***Reference Web Sites***

- **www.national.com/tempsensors**  
Temperature Sensors, Hardware Monitors
- **www.national.com/adc**  
Data Conversion
- **search.national.com**  
Knowledge Base
- **www.national.com/store**  
Evaluation Boards
- **analogU.national.com**  
Online Applications Information Training



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These are just a few of the popular offerings that National has on its website. The first two URLs have product information. The "Knowledge Base" area features an intelligent search feature where you can enter your question in natural language. Access to other areas, such as a cross-reference guides, can also be made from this page.

From our "store," you may purchase product evaluation boards.

Our Analog University offers additional on-line training in many areas.

Watch for expansion in all areas of our website.

# **ADC Glossary of Terms**

## A

**Absolute Maximum Ratings** – Voltages and currents beyond which a device may not be stressed without danger of damaging or destroying the device. The device is NOT guaranteed to work when stressed at or near its absolute maximum ratings.

**A/D** – See ADC.

**A/D Converter** – See ADC.

**A.C. Termination** – Transmission line termination technique where a series RC is used at the receiving end of a transmission line.

**ADC** – Analog-to-Digital Converter. A device or circuit used to convert analog information to digital words.

**Aliasing** – Conversion of an input frequency to another frequency as a result of the conversion process. The output frequency of an ADC can never exceed  $\frac{1}{2}$  the sampling frequency of the ADC without this aliasing. When the input frequency does exceed  $\frac{1}{2}$  the sampling frequency, the output frequency becomes the absolute value of  $[\text{INT}(f_{\text{IN}}/f_{\text{S}} + 0.5) * f_{\text{S}} - f_{\text{IN}}]$ .

## C

**Characteristic Impedance** - The impedance a transmission line such that, when driven by a circuit with that output impedance, the line appears to be of infinite length such that it will have no standing waves, no reflections from the end and a constant ratio of voltage to current at a given frequency at every point on the line.

## D

**DAC** – Digital-to-Analog Converter. A device or circuit used to convert digital words into analog voltages or currents.

**Director** – The shorter elements of a “Yagi” antenna that direct energy toward the driven element.

**DLE** – Differential Linearity Error. Same as DNL.

**DNL** – Differential Non-Linearity. The measure of the maximum deviation from the ideal step size of 1.00 LSB.

## E

**ENOB** – Effective Number Of Bits. A specification that helps to quantify dynamic performance. ENOB says that the converter performs as if it were a theoretically perfect converter with a resolution of ENOB. That is, an ENOB of 7.4 says that the converter performs, as far as SINAD is concerned, as if it were a perfectly ideal ADC with a resolution of 7.4 bits (assuming you could have fractional bits). The idea behind ENOB comes from the fact that the absolutely perfect ADC has an SNR that comes only from quantization noise and has absolutely no distortion. When this is the case, SINAD is then equal to SNR. Since SNR of the absolutely perfect ADC is  $\text{SNR} = 6.02 * n + 1.76$ , where “n” is the number of ADC output data bits,  $\text{SINAD} = \text{SNR}$  for a perfect converter, so  $\text{SINAD} = 6.02 * n + 1.76$  and  $n = (\text{SINAD} - 1.76) / 6.02$  and we say that  $\text{ENOB} = (\text{SINAD} - 1.76) / 6.02$ .



## ***ADC Glossary of Terms (2)***

### **F**

FFT – Fast Fourier Transform. The FFT is a mathematical operation that converts signals between the time and frequency domains. We generally call the frequency domain (amplitude vs. frequency) plot an FFT.

EMI/RFI – Electromagnetic Interference/Radio Frequency Interference. This is the radiation of EM (electromagnetic) energy that may interfere with other circuits and systems.

FR-4 – A glass epoxy printed circuit board material of woven glass cloth construction laminate with an epoxy resin binder.

Full-Scale Input Swing – The difference between the maximum and minimum input voltages that will produce a valid ADC output without going over- or under-range.

### **G**

Gain Error – The error in the slope of the ADC transfer characteristic. It is the difference in the actual and ideal full scale input range values.

### **I**

IMD – Intermodulation Distortion. This is the creation of new spectral components that result from two or more input frequencies modulating each other when the circuit is nonlinear.

ILE – Integral Linearity Error. This is the same as INL.

INL – Integral Non-Linearity. The maximum departure of the ADC transfer curve from the ideal transfer curve. INL is a measure of how straight the transfer function curve. There are two popular methods of measuring INL: End-Point and Best-Fit. The End-Point method is the most conservative, while the Best-Fit method gives lower (better-looking) values. National uses the End-Point method.

Input Dynamic Range – For an ADC, the range of voltages that can be applied to the input without going under-or over-range.

Input Offset – The difference between the input value of 1.0 LSB and the input voltage that causes the ADC output code to transition from zero to the first code.

Input Offset Error – The difference between the ideal input value of 0.5 LSB and the input voltage that causes the ADC output code to transition from zero to the first code.

### **J**

Jitter – The variation in the timing of a signal's rising or falling edge. It can be specified as cycle-to-cycle or long term.

### **L**

Loop Area – The area between the conductors of outgoing and return currents.

LSB – Least Significant Bit. The bit that has the least weight.

## **ADC Glossary of Terms (3)**

### M

Missing Codes – Those ADC codes that never appear at the ADC output. These codes can not be obtained with any input value.

### N

Nyquist Rate –The minimum sampling rate (or frequency) needed to prevent frequency aliasing.

Nyquist Frequency –The maximum input frequency beyond which frequency aliasing results.

### O

Offset Error – This is the same as Input Offset Error.

### P

PC Board or PCB – Printed Circuit Board.

Proximity Effect – The phenomenon whereby outgoing and return currents want to flow close to each other.

PSRR – Power Supply Rejection Ratio. A measure of how well a circuit rejects a signal on its power supply. There are two ways to specify PSRR, the most common of which is to specify the change in one parameter when the DC value of the power supply is changed. That is, one value of DC voltage is applied to the supply pins and the selected parameter (e.g. offset error) is measured. Then another DC voltage is applied to the supply pins and the same parameter is again measured. The extent to which the selected parameter does not change when the supply voltage is changed is the DC PSRR. This tells us nothing about how well an AC signal, such as noise, on the supply line will be rejected by the device.

The other method is to specify how an AC signal on the power supply will affect the output of the device. National specifies both methods for most of our ADCs. This provides the all-important AC PSRR, but also provides DC PSRR that may be compared with competition. Note, however, that the two readings have no relationship to each other.

### Q

Quantization – The process of dividing a range of analog voltages or currents into smaller “quanta” (smaller range of voltages or currents) such that each quanta is represented by a single digital code.

Quantization Error – The error introduced as a result of the quantization process. The amount of this error is a function of the resolution of the quantizer. By definition, the quantization error of an ADC is  $\frac{1}{2}$  LSB.

Quantization Noise – The noise at the ADC output that is caused by the quantization process. It is defined as  $20 * \log(2^{(n-1)} * \sqrt{6})$ , or about  $6.02 * n + 1.76$  dB, where “n” is the number of output bits of the ADC.

Quantizer – A circuit that carries out the quantization process. Another name for an analog-to-digital converter.

## **ADC Glossary of Terms (4)**

### R

**Reference Voltage** – For an ADC, the reference voltage is the voltage against which the analog input or an ADC is compared to determine the ADC output code. For a DAC, the reference voltage is multiplied with the ratio of the DAC input code to its (full-scale code + 1) to determine its analog output.

**Reflector** – The longer elements of a “Yagi” antenna that reflect energy back to the driven element.

**Resolution** – A measure of how well the ADC input is “resolved”, or how well the value of an LSB represents the analog input. Resolution is usually expressed in bits, and then indicates the number of bits available in the ADC output word.

The number of discrete output states or values of an ADC or a DAC, can also be expressed in the number of digital bits in the output (for ADCs) or the input (for DACs).

### S

**Sampling Noise** – The inherent noise of an ADC that comes from the steps in the transfer function.

**Scale Factor** – The effective multiplier of the analog reference voltage input to an ADC or DAC. This value is usually one, but can be any whole or fractional number.

**Series Termination** - Adding a resistor in series with a transmission line such that the driver-output impedance plus the resistance of this external resistor is equal to the characteristic impedance of the transmission line.

**S/(N+D)** – Signal-to-Noise Plus Distortion. See SINAD.

**SINAD** – Signal-to-Noise And Distortion ratio. A combination of the SNR and THD specifications, SINAD is defined as the rms value of the fundamental signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding DC. SINAD can be calculated from SNR and THD. Because it compares all undesired frequency components at the output with desired frequency. It is an overall measure of the dynamic performance of the ADC. SINAD is also known as SNDR, S/(N+D) and Signal-to-Noise Plus Distortion.

**Skin Effect** – The phenomenon by which high-frequency current flow is restricted to the surface, or skin, of a conductor.

**SNDR** – Signal-to-Noise And Distortion Ratio. See SINAD.

**SNR** – Signal-to-Noise Ratio. The ratio of the power in the signal to the power in all other spectral components below ½ the sampling frequency, excluding harmonics and DC.

**Split Ground Plane** – Concept where analog and digital grounds are in a single PCB layer and only connected at a single point.

**Substrate** – The base semiconductor material upon which solid-state devices are built. The substrate is resistive with a resistance that is on the order of a few Ohms.



## ***ADC Glossary of Terms (5)***

### **T**

THD – Total Harmonic Distortion. The ratio of the rms total of a specified number of harmonic components to the rms value of the output signal. National uses the first nine harmonics ( $f_2$  through  $f_{10}$ ).

Through Hole – The hole that goes through a printed circuit board to connect together lines and/or planes in two or more layers.

### **V**

$V_{REF}$  – See “Reference Voltage”.

### **Z**

$Z_O$  – The characteristic impedance of a transmission line.





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## **DATA TRANSMISSION**

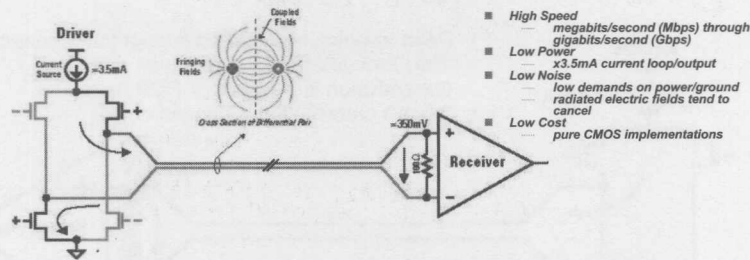
Communications Interface Division

## **What Is LVDS?**

The next section covers LVDS (Low Voltage Differential Signaling) circuit basics.

*James.chang@nsc.com.  
Wrong slide 1 of 2 amps.*

# What Is LVDS?



- **High Speed**  
— megabits/second (Mbps) through gigabits/second (Gbps)
- **Low Power**  
—  $\sim 3.5\text{mA}$  current loop/output
- **Low Noise**  
— low demands on power/ground  
— radiated electric fields tend to cancel
- **Low Cost**  
— pure CMOS implementations

- **Low Voltage Differential Signaling (LVDS)**
- **ANSI/TIA/EIA-644-A-2001 Standard**
  - Only electrical levels specified
  - Medium independent
  - Other standards reference LVDS
- **Also standardized by IEEE for use in SCI**
  - IEEE 1596.3 (1995) (similar, not identical)
- **Gigabits/second (Gbps) at milliwatts over backplanes or up to 10-15m cable**

**Gigabits**  
@ milliwatts

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Low Voltage Differential Signaling (LVDS) is specified in standard ANSI/TIA/EIA-644-A-2001 (this is a revision of past ANSI/TIA/EIA-644 versions). This standard specifies LVDS electrical signaling levels only— transmission medium and application are up to the user, making LVDS useful in a wide variety of applications. In fact, many system standards refer to LVDS for the signaling scheme.

The TIA version is a generic standard specifying only the driver-output and receiver-input characteristics. It is intended to be referenced by other standards that define the complete interface including protocol, connectors, and media such as the Camera Link standard or the FPD Interface standard for notebooks specified by the SPWG (Standard Panels Working Group). It is also used in many proprietary applications.

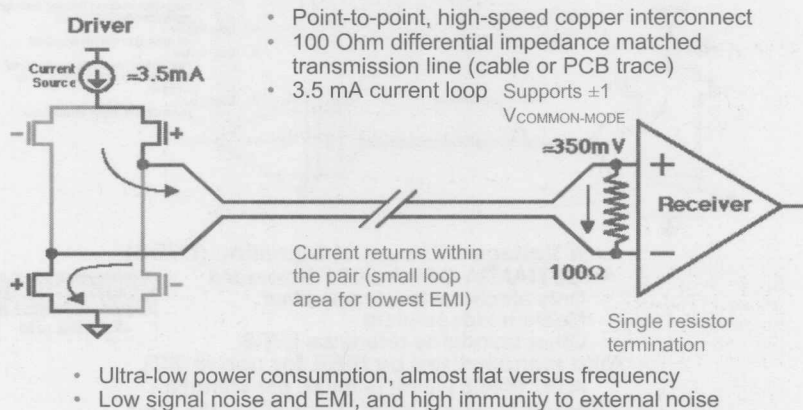
The IEEE standard specifies LVDS for an SCI application (Scaleable Coherent Interface) and varies in tests, conditions, and limits. This is more of a specific vertical application, but conceptually they are the same.

LVDS is a current-loop signaling technology in which the current-loop direction (clockwise or counter-clockwise) determines the logic level (high or low). Approximately 3.5 mA is driven down one wire of the pair and returns through the other wire of the pair. A voltage (approx.  $\pm 3.5\text{ mA} \times 100\Omega = \pm 350\text{ mV}$ ) is generated across the termination resistor.

The receiver, a differential comparator, measures the polarity of this voltage drop, positive voltage corresponding to logic high and negative voltage to logic low.

The small swing, differential nature of LVDS makes it a high-speed, low-noise, and low-power technology. Relatively constant, small output current lowers power/ground noise and since the current in the signal pair is a closely-coupled current loop, fringing electric fields tend to cancel, reducing EMI.

## LVDS Circuit Basics



- Ultra-low power consumption, almost flat versus frequency
- Low signal noise and EMI, and high immunity to external noise



4



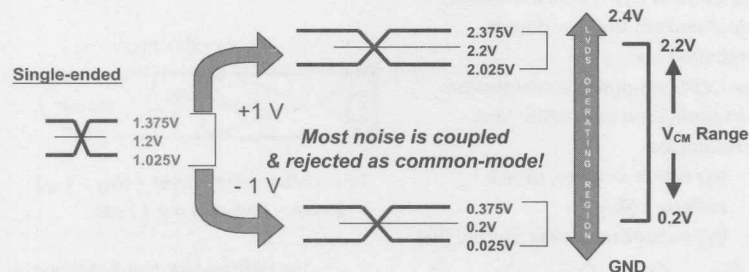
This is a simplified view of how a low-voltage, differential signaling technology works. Current flows through the terminating resistor and the receiving device interprets the voltage across the resistor. Based on the difference in voltage across the resistor, the receiver will signal a full-level CMOS/TTL 1 or 0.

The connection should be treated as a transmission line – with ever increasing care as the distance increases. Because of the low-voltage nature of this technology and potential EMI implications, LVDS is primarily useful for short-haul distances of only a few meters.

However, because this line is differential, the signal is immune to a lot of interference, using common-mode rejection. Another main benefit comes from the low power consumption. Given the low current, only small amounts of power are consumed during operation.

Most National LVDS devices support any common-mode voltage inside the devices VDD and GND power connections. See the individual datasheets for information specific to each part.

## LVDS Common-mode Range



Driver Differential Output Voltage	$V_{OD}$	250 - 450 mV
Driver Offset Voltage	$V_{OS}$	+1.25 V
Receiver Thresholds	$V_{TH}$	$\pm 100$ mV
Receiver Input Voltage Range	$V_{IN}$	GND to +2.4 V
Common-Mode Range	$V_{CM}$	$\pm 1$ V around 1.25 V
Differential Noise Margin	DNM	150 mV
Data Rate Range	$f$	DC to ~2Gbps
Cable Length Range	$L$	0 to ~15+ meters



See ANSI/TIA/EIA-644-A-2001 for complete specifications.

5



For LVDS, the common-mode voltage ( $V_{cm}$ ) should be compared to single-ended noise margins (ie 400 mV for BTL). Noise will be picked up as common, if closely-coupled differential pairs have been used on the interconnect.

At  $\pm 1$ V, LVDS and Bus LVDS have more than twice the noise margin as low-swing BTL or GTL devices.

The  $\pm 1$   $V_{CM}$  also provides for hot/live insertion capability.

LVDS is very robust –

Signal =  $\pm 400$  mV, Noise =  $\pm 1000$  mV, N/S = 2.5

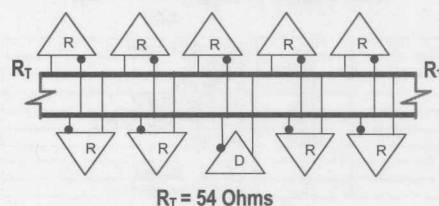
For CMOS we have –

Signal = 3000 mV, Noise = 400 mV, N/S = 0.133

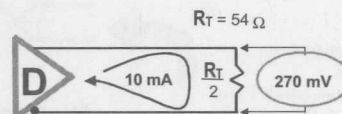
LVDS Noise-to-Signal ratio is 18 times better than CMOS!

## What Is Bus LVDS / Why Do We Need It?

- Bus LVDS is LVDS with increased output current to drive double-terminated buses
- Bus LVDS simplifies transmission line termination over other bus technologies
  - **NO** active devices, only 2 resistors ( $R_T$ )
  - **NO** secondary power supply ( $V_T$ )



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$$\begin{aligned} \text{Termination Load Power} &= (I_{OD} \times V_{OD}) \\ &= (10 \text{ mA} \times 270 \text{ mV}) = \underline{2.7 \text{ mW}} \end{aligned}$$

- Bus LVDS products have fault tolerance:
  - High impedance on power down
  - Hot insertion capability
  - Bus contention tolerance
- Bus LVDS features
  - Light bus loading (< 5 pF)
  - Balanced output impedance (Do-/Do+)
- Ruggedness
  - > 2000 V ESD to HBM
  - > +/- 300 mA latch up

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When it comes to overall system power benefits, there is no bus-driving technology that can compare with Bus LVDS. Bus LVDS has the lowest power consumption on chip because of the constant bus driving current of 4 to 10 mA. It can drive a heavily loaded bus with only 10 mA because it also minimizes the bus loading from other transceivers attached to the bus. Another big benefit to the overall system is the low cost of termination and the low power dissipated at the termination.

Bus LVDS does not require any active devices for the termination. Unlike GTL, SSTL, or TTL, Bus LVDS in a multidrop configuration only uses two passive termination resistors. All other bus-driving technologies require a tightly regulated termination voltage, such as 1.5V for GTL+. This tight regulation adds substantial cost to the backplane design because of the required voltage control chips and passive components to surround the chips. However, why add voltage regulation when Bus LVDS only requires that you have 2 resistors?

A bus designer will determine the Bus LVDS termination resistor ( $R_T$ ) value by calculating the loaded impedance ( $Z_L$ ) of the bus. There are complex sets of variables that determine the  $Z_L$ . The factors are the spacing between the loads—or plug-in cards—and the characteristic impedance ( $Z_O$ ) of the backplane trace. In addition, the loading from the plug-in card stubs, connectors, and transceiver loading affect the  $Z_L$ .

For example, a designer determines the  $R_T$  value for a backplane by analyzing the variables. A complete description on how to do this is available on the [lvds.national.com](http://lvds.national.com) Web page.

For understanding purposes only—and not an actual calculation—assume a backplane with  $Z_O$  = 100 Ohm with 30 mm spacing between 20 slots, 30 mm stub lengths, 2 mm style connectors, and National's DS92LV010 Bus LVDS transceiver on all cards. In this case, the  $Z_L$  is about 54 Ohm and is terminated at both ends with half of this value. This is shown above.

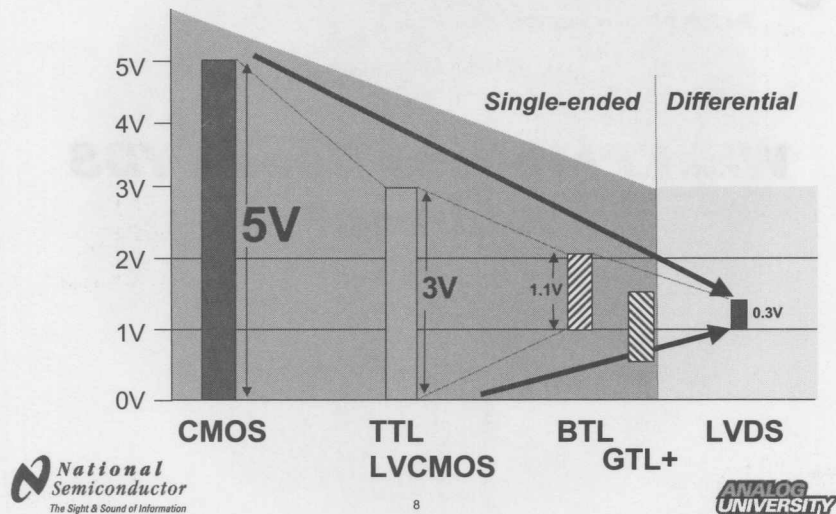
The load power calculation shows the loop current multiplied by the voltage drop across the  $R_T$  as the power dissipated at the terminations. The 10 mA output current flows through the equivalent  $R_T$  divided by 2 value of 27 Ohm with the result of 2.7 mW total power per differential bus line. The 2.7 mW is an order of magnitude less power than any other bus technology's termination power dissipation.



## **What Problems Does LVDS Address?**

The next section addresses problems commonly solved by using LVDS technology.

## Migration to Low Swings



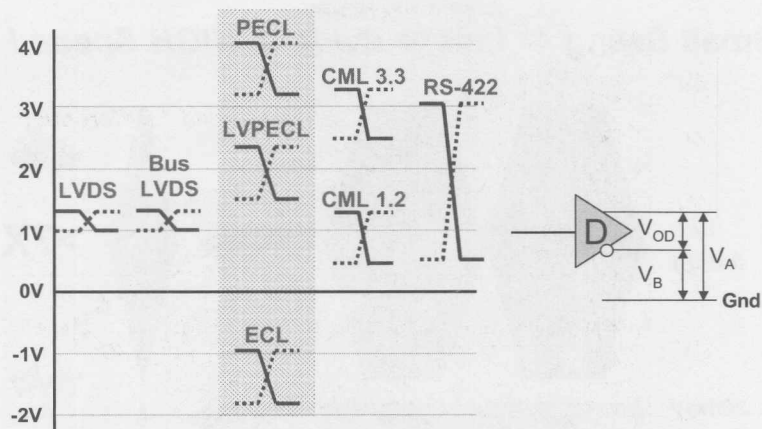
The need for speed is real and increasing at a tremendous rate every year. As processors get faster and faster, bus speeds increase to service them. As speed goes up, the timing margins shrink – thus the need for high-performance interface devices. Remember the days of text-only messages? Today you get icons, images, and loads of attachments on every email – thus the demand for bandwidth is pushed from the desktop through the datacom and telecom networks.

This slide shows the trend to smaller swings and also the conversion to differential. Typically when reducing signal swing, noise margin is also reduced. However, this is not the case with LVDS, even though it has a smaller swing than BTL or GTL. It offers more noise margin. This is the benefit that the differential transmission scheme provides.

The use of TTL/CMOS logic or reduced swing technology (BTL and GTL) for backplanes is today's common choice for design engineers, although they both lack providing the level of noise immunity that LVDS signaling offers, consume too much power, have complex terminations, and suffer a clear migration path.



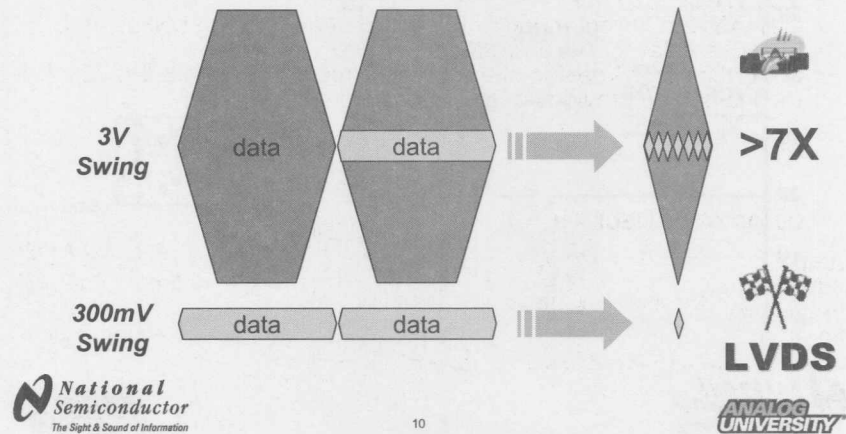
## Differential I/O Comparisons



This slide shows the typical levels of common differential transmission technologies. LVDS features the smallest swing, and with a low offset, it is more compatible with low voltage power supplies which are becoming more common every day. In order for CML to maintain interoperability between supply levels, AC coupling must be employed.

## High Speed Operation

Small Swing  $\Leftrightarrow$  fast  $\Leftrightarrow$   $dv/dt$   $\Leftrightarrow$  HIGH Speed !



SPEED – the transition time of a signal is a limit of how fast you can go. A larger signal swing will take a longer time to transition. One solution to go faster is to decrease the transition time, but that is not practical due to noise, crosstalk, EMI and power reasons.

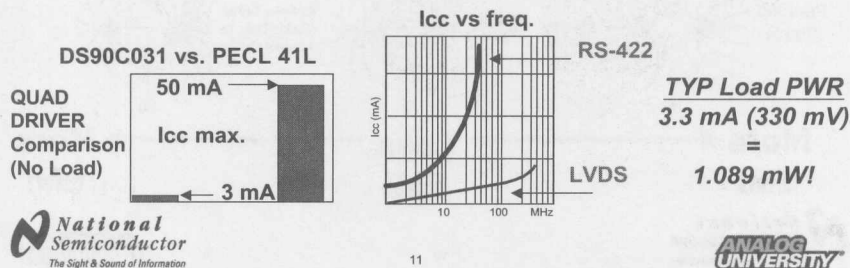
To gain speed, LVDS speeds up transition time by lowering the signal swing. The faster transition times do not increase crosstalk, EMI, and power because of much smaller signal swings. Typically this also reduces noise margins, but LVDS solves this problem with its differential transmission scheme where the signal-to-noise ratio is greatly improved.

The graphic above illustrates that with a small signal 1/10 of the large one, a better than 7X speed improvement is obtained with the same  $dv/dt$ . But that is not all, with the small signal, increasing the  $dv/dt$  is now possible and even higher speeds are obtainable!

LVDS gains its speed due to the small signal swing..... and this helps other desirable benefits like power and less noise.

## Ultra Low-Power Dissipation

- **LOAD:** Small load current, 3.3 mA! (330 mV/100Ω) => Low load power: ~1.1 mW!
- **VOLTAGE:** 330 mV
- **DYNAMIC:** Current-mode driver minimizes switching spikes and provides a flat " $I_{CC}$  vs. Frequency" curve
- **STATIC:** CMOS design of the driver & receiver cell (0.8 & 0.35 technologies), provides a low  $I_{CC}$  current



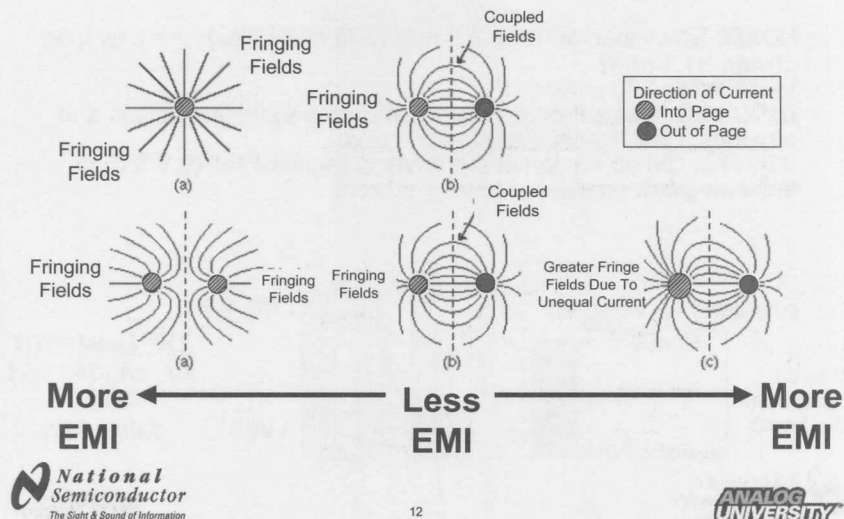
One of the primary goals of LVDS is LOW POWER dissipation. This has been achieved by using a CMOS process to minimize static current draw. The driver design is current-mode, thus switching spikes are greatly reduced. This lowers EMI and simplifies power distribution and bypassing requirements. Also the  $I_{CC}$  vs frequency curve is very flat. For a voltage-mode driver on the other hand, power supply current ( $I_{CC}$ ) dramatically increases with frequency and thus the device is typically limited to <50 MHz operation. Using a differential data-transmission scheme, the load voltage can be reduced while still providing  $\pm 1V$  of noise rejection (common-mode). This allows for a reduction in  $V_{od}$  (2 V min. for 422, and 800 mV for PECL) to 330 mV (LVDS). Even with a 300 ps transition time, slew rate is kept to about 1V/ns. With 330mV across the 100 Ohm load, a load current of only 3.3 mA is required, compared to >20 mA for 422. LVDS addresses static and load current, providing the lowest power interface and enabling higher levels of integration without heat slugs hidden in the packages!

Four words to remember:

Load  
 Voltage  
 Dynamic  
 Static

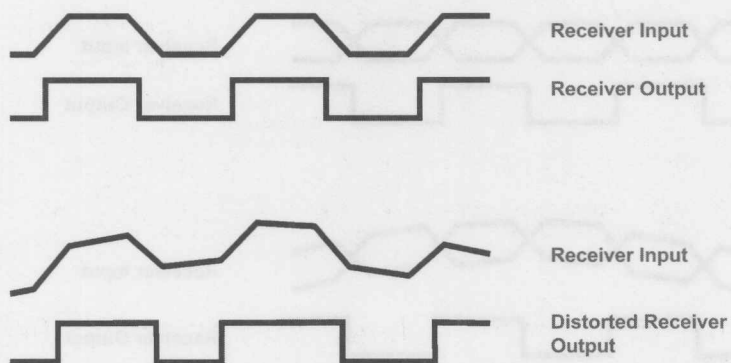
and LVDS minimizes power in all of them!

## EMI & Differential Traces



This slide shows basic EMI fields. A single line in space emits fields. When true differential data transmission is employed, two lines are used. Current flows in opposite directions and the fields tie up and cancel each other. This slide graphically shows the importance of the distance between the pairs. When common-mode noise is on the line, there is an unequal current flow in the pair, and the increased emissions can be seen. For noise minimization, the transmission mode should be pure differential, and the lines should be close together. This helps ensure that noise picked up will be coupled as common-mode and rejected by the receiver. And as we will see on the next foils, by closely-coupling the lines, the fields tend to tie up more and therefore radiate less.

## ***Common-Mode Noise Single-Ended Signals***



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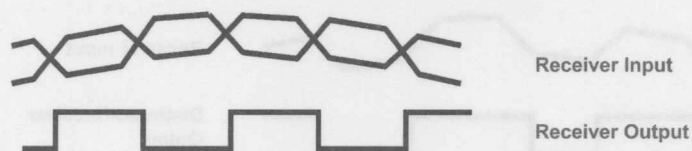
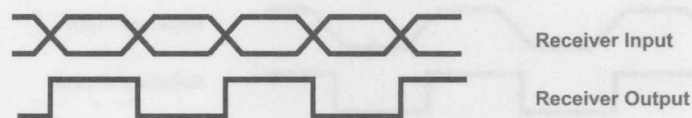
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Common-mode noise on single-ended signaling can be interpreted as pulse width distortion by the receiver, reducing timing margins.

## **Common-Mode Noise**

### **Differential Signals**



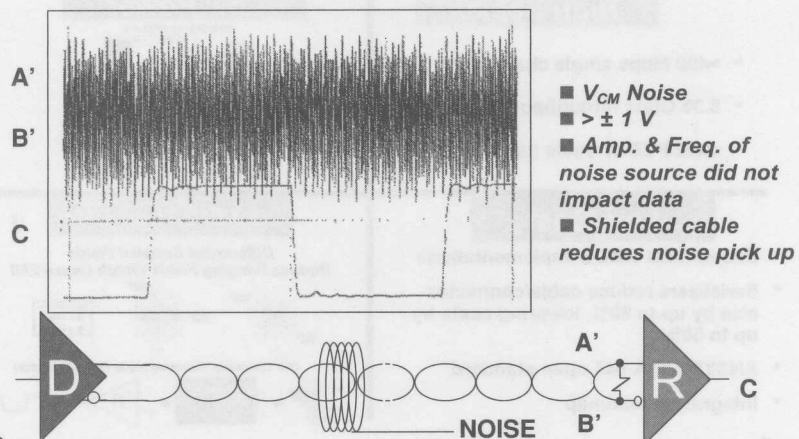
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Common-mode noise on differential signals is rejected by the receiver, minimizing performance impacts.

## Common-Mode Rejection



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Common-mode noise has been coupled on to the LVDS signals (top waveforms: A' & B' both are plotted together). The bottom waveform is the receiver output signal (C). The receiver rejects common-mode noise, and only responds to the differential signal carrying the digital information. LVDS is required to provide a minimum of  $\pm 1$  V (GND to +2.4 V) of common-mode rejection. Most receivers provide more, typically -0.5 V to ( $V_{cc} + 0.5$  V) before clamping by the internal ESD structures occurs. In the plot above, greater than  $\pm 1.5$  V common-mode noise is being applied.

## LVDS / BusLVDS Advantages

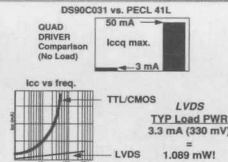
### High Speed

- >400 Mbps single channel
- 6.38 Gbps throughput chipsets
- Over PCB or cable (up to 15m)

### Low Cost

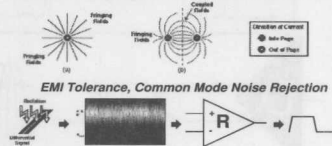
- Economical CMOS implementations
- Serializers reduce cable/connector size by up to 80%, lowering costs by up to 50%
- ANSI/TIA/EIA-644 open standard
- Integration roadmap

### Low Power



### Low EMI/High CMR

Differential Coupled Fields  
Reduce Fringing Fields Which Cause EMI



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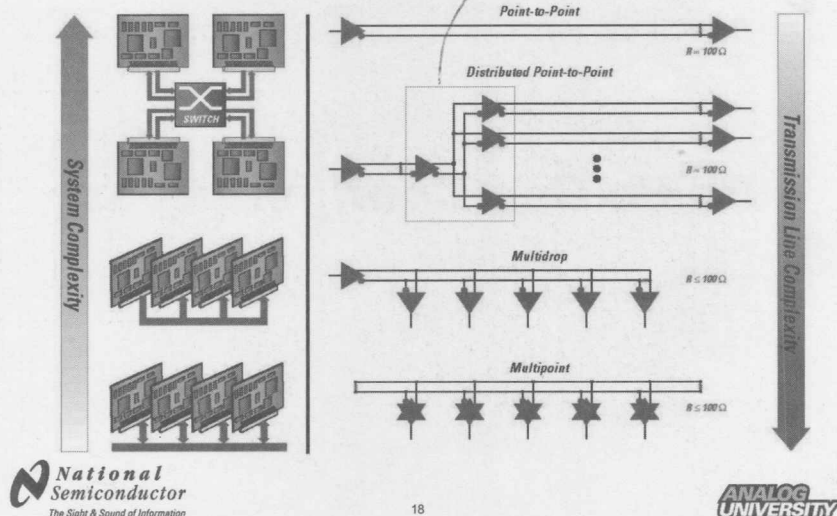
To summarize, LVDS increases speeds, reduces power consumption, lowers system cost, and lowers EMI.



## **Basic Bus Configurations**

The next section discusses the most common basic Bus configurations.

## Bus Configurations Trade-Offs



LVDS is primarily intended for use in dedicated high-speed point-to-point links. However, it also can be used in other configurations (multi-drop for example) if the interconnection supports the required signal quality (no reflections off the mid-cable nodes or stubs, and only one termination, etc).

Termination is required by the current-mode driver and should be selected to match the characteristic (differential-mode) impedance of the cable. This will provide the best signal quality and minimize reflections and emissions. The interconnecting media is an important part of the system and should provide adequate balance to maintain signal quality (i.e. twisted pairs).

The simplest is a single-direction point-to-point bus. This is the main configuration of standard "LVDS" devices. Note: only one termination resistor is required at the far end of the cable, and the driver is always located at the opposite end. If this configuration is employed and communication needs to occur in both directions, then a separate path is required (2 pairs). At the expense of twice the interconnect, simultaneous transmission can occur and twice the throughput of the shared bus is obtained.

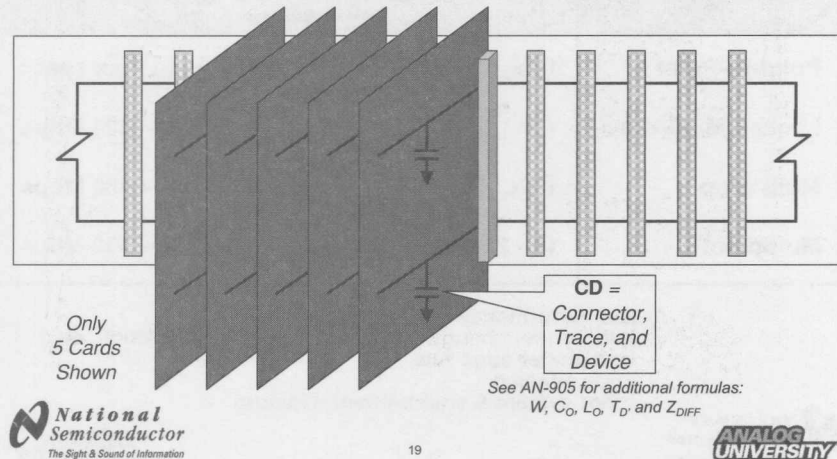
Another popular configuration is the classical distribution system or multi-drop bus. Once again, communication is in a single direction, termination is at one end only, and the driver is located at the other. On high-speed buses, the connection of multiple receivers needs to be done with care to preserve the signal quality of the line.

The most flexible configuration is the multipoint or shared bus configuration. Termination is at both ends of the the interconnect, and the driver may be located anywhere on the bus. Only one driver can be active at a time (normal mode), so transmission is bi-directional half-duplex. The connection of nodes to the bus is critical and needs to be done with care.

For double-terminated applications, multi-drop with the driver in the middle or multipoint, BLVDS, or multi-point drivers should be used due to their increased output drive current. They are designed to provide LVDS-like swings while driving loads in the 30 to 50 Ohm range.

## Loaded Bus Impedance

Distributed capacitance load lowers  $Z_0$



This slide shows a differential bus with five cards plugged in. The card shown adds a load to the bus mainly composed of a bulk capacitance load (CD) resulting from the connector (2-3 pF), the PCB trace (2-3 pF), and the device (4-5 pF), for a total load of about 10 pF. Limit the number of vias on the card's stub to minimize capacitance loading. Keep stub length as short as possible. These two tips will help to maintain a high "loaded" bus impedance that will increase noise margins.

Certain Bus LVDS devices are capable of operating in wild-card configurations! Depending upon system noise margin goals, full card loading is NOT required. Termination selection is a bit tricky, but should be matched to a fully loaded case (or slightly higher). Waveshape is good even for half loaded or section loaded buses! Single-ended technologies cannot support this feature due to noise margin violations.

## General Bus Performance

Topology	Configuration	Performance
Point-to-Point	1 Tx, 1 Rx	Up to chip max spec
Limited Multi-drop	1Tx, 2 - 4 Rx	Up to 500 – 600 Mbps
Multi-drop	1 Tx, 10 - 20 Rx	Up to 300 – 400 Mbps
Multipoint	10 - 20 Transceivers	Up to 200 – 300 Mbps

- Actual performance varies and depends on
  - interconnect bandwidth (impedance control, stubs, etc.)
  - transmitter edge rate
  - node spacing
  - other system & environmental factors



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In general:

- Point-to-point links can be operated up to the chipset maximum specification, depending if the interconnect can support the speed.
- Some devices can be used in multi-drop configurations, depending on output edge rates, stub lengths, number of loads, load spacing, etc.
- Multipoint is limited to Bus LVDS and M-LVDS bus transceivers.

## ***Life at the Sharp End***

### **The start of the signal-path processing is... the Operational Amplifier**



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Many signal paths start with that most universal of analog components, the operational amplifier\*. First named for its ability to perform mathematical operations (addition, subtraction, integration, differentiation etc) the modern Op-Amp provides the interface to many transducers and sensors, starting the process of converting real-world sensations such as sound, temperature, pressure, and light into electrical signals. Many signal sources simply require amplification or buffering, while others require manipulation to correct transducer or transmission errors. Op-Amps often can combine many of these functions, because the transfer characteristic of an Op-Amp is determined primarily by the external components connected around the Op-Amp.

Despite the fact that the Op-Amp is essentially a five-terminal device, with two input pins, two supply pins (or supply and ground), and one output pin, there are literally hundreds of Op-Amp types. National alone has more than 300 different types of Op-Amp, not counting duals, triples, and quads as separate types, and other manufacturers have similarly large portfolios.

During this seminar we will take a look at the characteristics that distinguish these Op-Amp types, why they are different, and how to choose the "right" Op-Amp. Techniques for solving common Op-Amp problems will be described, along with practical circuit applications.

The Op-Amp is only the first part of the signal path. Later on we will show how to accurately convert the signal to a digital format and then transfer that digital data, again without errors, to a storage or processing medium.

However, that is not where the signal path ends. Very often the signal information needs to be put back into a way that we in the "real world" can comprehend, either directly from the source or from the storage medium. Closing the circle, Op-Amps or their cousins are used to drive speakers, display devices, motors and RF transmitters.

\* A notable exception is RF receivers.



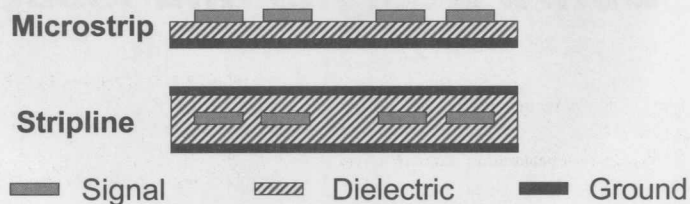
## **Board Designs and Issues**

The next section addresses some common backplane design issues commonly addressed by using LVDS technology.



## PCB Traces

- **Microstrip (Outside)**
  - Higher impedance range
  - No VIA loading
  - Less options
  - Less shielding
- **Stripline**
  - More options / density
  - More shielding



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There are many decisions to be made when selecting which type of trace will be used for an interconnect. The two most common structures employed are microstrip and stripline. Microstrip traces are laid out on the outside layers of the board (top or bottom), while stripline traces are embedded in the board, typically between planes as shown above.

Microstrip offers high impedance structures and may not require any vias that can adversely load down a signal (cap. loading effect). Limitations of the microstrip line are less inherent shielding, and the fact that in a multi-layer board, there are only two layers for microstrip traces (top and bottom). National's first Proto BLVDS backplane used microstrip traces. Typical differential-trace maximum impedance is about 150 ohms for microstrip (but is dimension and material property specific).

Stripline offers more shielding, and depending upon the number of layers in the board (or backplane), more routing channel options in high-density applications. The down side of striplines is the required via to gain access to that plane and also the fact that it is more difficult to obtain high-impedance traces. Typical differential maximum impedance is about 130 Ohms for stripline (but is dimension and material specific). Some technical papers state that a 10 dB shielding effect is gained with striplines over microstrip.



## Differential Pair Layout Options

- Edge-coupled differential pair
  - More control of "S" ( $S < h$ )
  - Requires 2 routing channels
  - Stripline (shown) or Microstrip
- Broadside differential pair
  - Limited "S" options
  - Requires only 1 routing channel
  - Stripline only



Edge-Coupled



Broadside-Coupled

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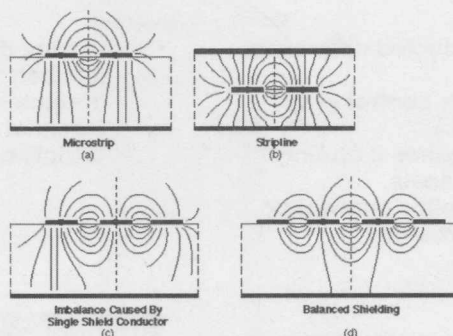
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There are two basic types of differential traces. For differential traces, the two lines should be routed together as close as manufacturing limits allow. This is done for two reasons. The first is for maximizing common-mode rejection. Coupled-noise amplitude is proportional to distance from noise source to victim. Keeping the lines together helps to ensure that the noise is coupled as common and is then rejected by the receivers. The second reason is related to the field-canceling effects. Keeping the traces close together ties up the generated fields better, allowing less energy to escape as noise. (See LVDS Owners Manual for test data).

Edge-coupled lines are more flexible since the distance between the lines is a design parameter. They can be designed as microstrip or stripline traces. It is also recommended to keep the distance "S" less than "h" to maximize coupling between the pair and not with the planes. Two routing channels are required for edge-coupled differential traces.

The other option is broad-side coupling. The distance between the pairs in this case is a material dimension (core or prepreg). This somewhat limits the impedance of the line, as "S" is not too flexible. Connector routing is also not as straight forward with this option.

## EMI of Microstrip vs Striplines



- Striplines offer more shielding due to the encasement of the lines between the ground planes
- A few industry papers site 5 to 10 dB reduction for striplines vs microstrip lines (single-ended)
- Closely-coupled microstrips to minimize EMI

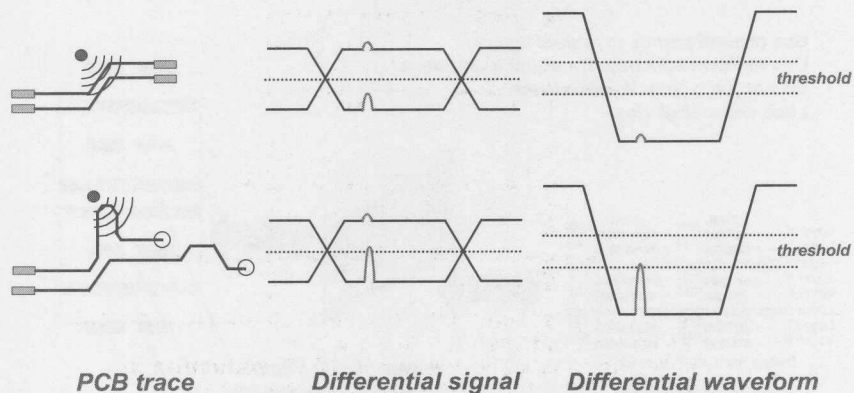
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Stripline offers better shielding than microstrip, but it is harder to get the desired differential impedance, potentially adds complexity (number of layers), requires vias, and thus increases cost. Therefore, microstrip is usually preferred if you are only routing a few pairs.

## Coupling & EMI



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The dot on the left is a noise source – the meandering effect is in-balance on the pair and more noise is picked up on one side, thus creating some differential noise. Solutions here would include: locating the noise source further away, meander less often for more balance, interconnect with striplines, or to employ the zero-skew connectors.

## Board/Backplane Stack-Up

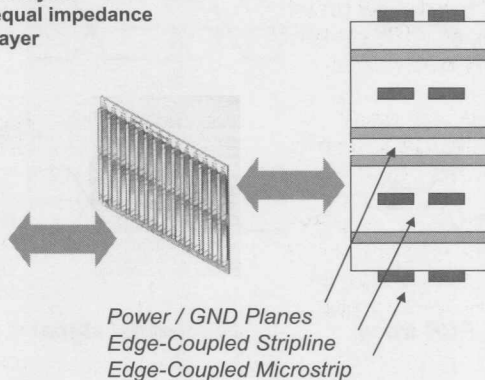
- Use ground planes to isolate layers
- Use uniform spacings for equal impedance
- Do not jump from layer-to-layer
- Limit number of vias

Layer 1	5 mil	81Ω	8 mil	69Ω
Layer 2		55Ω		43Ω
Layer 3				
Layer 4		42Ω		33Ω
Layer 5		42Ω		33Ω
Layer 6				
Layer 7		55Ω		43Ω
Layer 8		81Ω		69Ω

Dielectrics = .005",  $\epsilon_r = 4.1$

Source: SMT Plus., and Ritch Tech  
High Speed PCB Design, August 1993

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Now that trace impedance has been discussed, board stack can now be addressed. Here are some simple things to remember and some general guidelines:

- Narrower traces provide higher impedance lines.
- Microstrip lines can provide higher impedance than striplines.

### General guidelines:

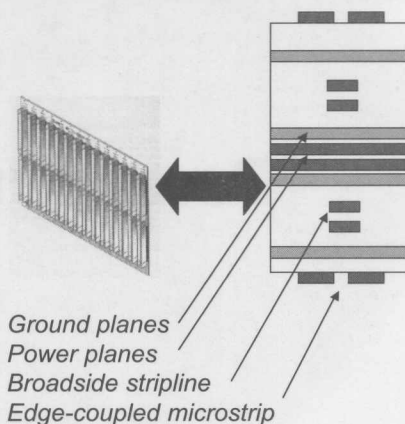
- Avoid unnecessary layer changes (via loading and impedance changes).
- For a parallel bus, use the same layer for all lines.
- Use symmetrical traces for equal loading.
- Consider impedance prior to selecting stack up.

### Trends

- Thinner lines (smaller W) have higher impedance.
- Larger heights (larger h) have higher impedance.
- Micro > Strip.

## Board/Backplane Stack-Up

- **Broadside lines:** best with ground on both side
- **Locate near outside if using blind via**
- **Power - ground plane spacing if minimized can make a great bypass**



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This slide provides additional data on stack up. Note that it is better to run the strip lines between ground planes (on both sides). This provides a nearby return path for any common-mode return currents. You can also obtain an excellent high-frequency bypass capacitance by using thin spacing between the power and ground planes.

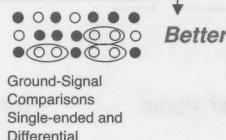
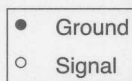
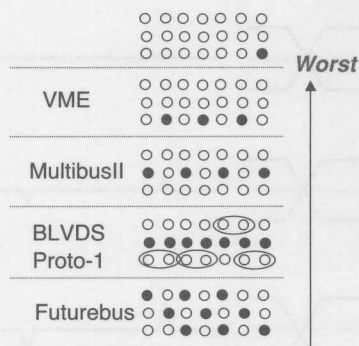
*Minimize inter layer distance  
- decoupling*

# Connectors

The next section addresses connectors and their importance in differential signaling.

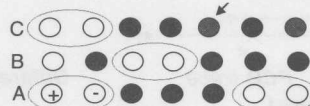
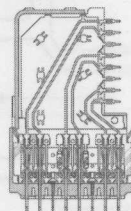
# Connector Pin Assignment

## Standard Matrix Connectors



- Route diff. pairs on same row
- Use shorter rows (A) or (B)
- Use GND pins to isolate TTL from BLVDS lines
- Special differential connectors are available

Teradyne Drawing and Photo of VHDM - HSD Connector



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Connectors are a complex topic and are the subject of many wars at standards committee meetings. There are two basic types: standard matrix-based connectors (3 rows of 32 pins) and special connectors. The special connectors have elaborate techniques to clamp to the PCB and are stealth-like to a TDR! They are also very application specific and tend to be rather expensive.

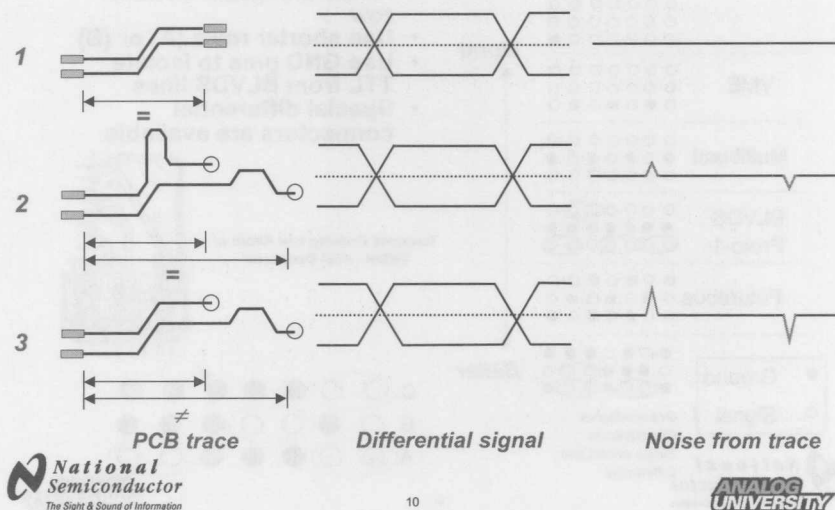
More common is the use of standard connectors for a mix of differential, power, ground, and single-ended connections. The above slide shows a variety of pinout recommendations for single-ended and differential options. The BLVDS Prototype backplane connector layout is also shown.

For differential lines in a matrix connector, adjacent pins in a row is best. The row with the shorter path provides a better path over the longer row also.

Ground signal assignment can be used to isolate large-swing (TTL) signals from the small-swing lines as shown above.



## Connector Skew Effects



The benefit of the zero-skew connectors is shown above. With equal lengths, skew is minimized and the line is in balance. 3M has a very good connector system that is right-angle, and very low skew.

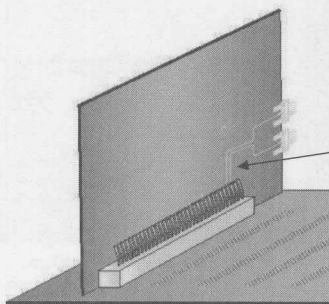
With a right-angle (dual row) connector, meandering one of the lines to deskew the pair may be required. This helps to minimize the common-mode modulation but is not optimized for balance (see next slide). Another solution would be to assign the pair to the same row. For a parallel bus application, another good trick is to enter on the long row and exit (at the other end) on the shorter row to balance the length of the pairs in a parallel bus (Channel Link).

The bottom illustration shows the impact if the line is not deskewed within the pair.



## Crosstalk

- Most backplanes have one or two pairs of signals that interfere with each other
  - This typically occurs at connectors
  - It can occur in the backplane by a discontinuity, for example a via



**As more pairs are added, crosstalk typically occurs in connectors but can also occur in the backplane**

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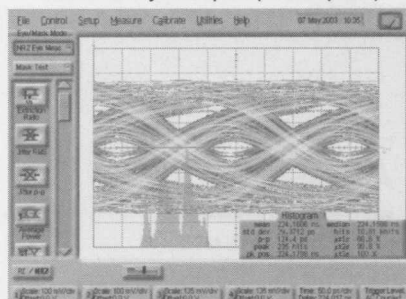
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Lower-cost connectors are common in existing applications. With the addition of multiple signals, smaller signal swings, and higher data rates, crosstalk is of great concern. Careful layout of signals through connectors becomes more critical. Please reference the LVDS Owner's Manual for guidance in routing signals through connectors.

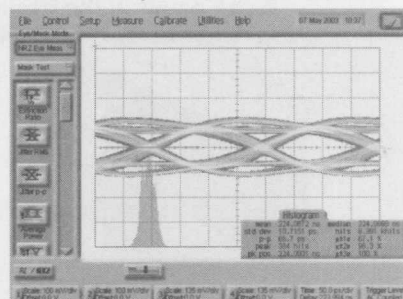
## De-emphasis Feature

After 16" of a Tyco backplane (no de-emphasis)



0.62 UI of Jitter with PRBS-7 Pattern

After 16" of a Tyco backplane with de-emphasis



0.33 UI of Jitter with PRBS-7 Pattern

De-emphasis not only helps reduce crosstalk but also reduces the DJ caused by the backplane.



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De-emphasis is a feature used to help reduce crosstalk and DJ through connectors and backplanes. However, because de-emphasis conditions the amplitude of the signal to be lower, it may not be suitable for use in very lossy long backplanes or cables without additional signal conditioning at the receive end.

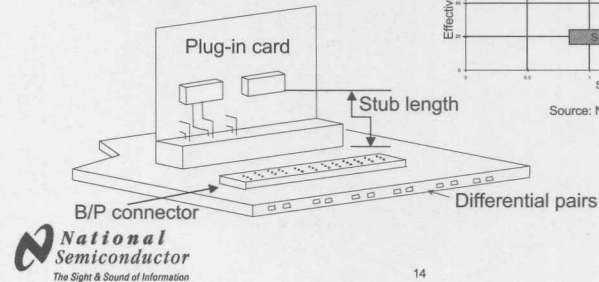
## **Stubs**

The next section talks about the effects of stubs on the signals.

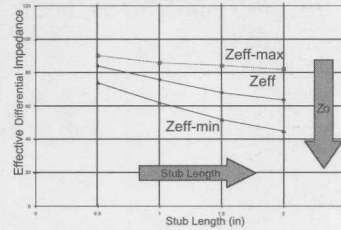
A stub is the distance between the backplane trace and the individual device load on a plug-in board. The stub length includes the connector, the trace to the integrated circuit, and the bond wire within the IC package.

## Stub Length

- The shorter the better!
- T-Line effects worsen with length
- Limit to 1.5" or less
- Priority to XCVR placement on card



The TDR Simulated Differential Impedance of 20 Slot, Full Loaded BLVDS Backplane with Differential  $Z_0=130$  ohms



Source: NESA BLVDS White Paper

Stubs - one golden rule:

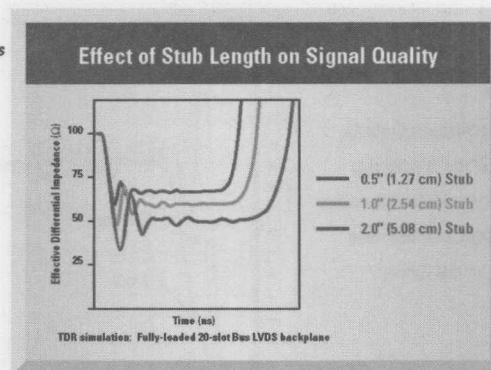
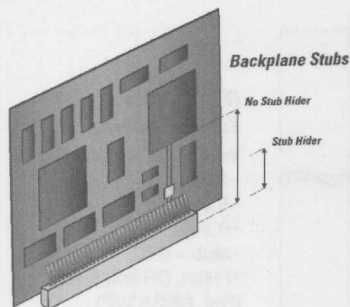
***The shorter the better!***

A long stub adds to the capacitance load and will lower the loaded impedance even more. To minimize the electrical distance and capacitance, a stub interconnect should be microstrip and the number of vias (0-1 is best) should be limited. The graph above is from the NESA White Paper on BLVDS and illustrates how increasing stub length lowers the loaded impedance. Stub length should be typically 1" or less.

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## Stubs Hider Application

- Stubs > 3 cm reduce large backplane performance to < 200 Mbps
- Small "stub hider" buffer can achieve < 3 cm stubs



Source: NESA Technical DesignCon99 Whitepaper: Signal Integrity and Validation of National's Bus LVDS Technology in Heavily Loaded Backplanes, [www.national.com/lvds](http://www.national.com/lvds)



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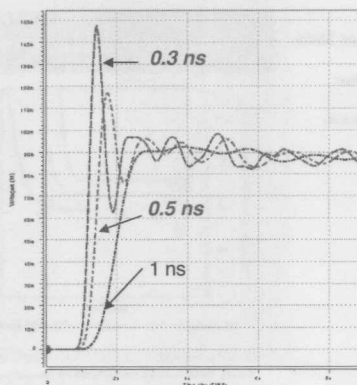
The NESA DesignCon99 White Paper ([www.national.com/lvds](http://www.national.com/lvds)) simulates backplane performance versus stub length and other parameters. As shown in the TDR (Time Domain Reflectometry) plot above, with a 2.0' (5.08 cm) stub length, the effective differential impedance drops to almost 30 Ohms.

Even if you've designed in the world's best LVDS device, you may not be able to place it close to the connector. In multi-drop and multipoint system topologies, short stub lengths are necessary to minimize reflections. In these systems, stub length has a large impact on signal quality and often is the main factor determining maximum bus speed. When running at 200 Mbps, edge rates will be fast enough to require stubs less than 2-3 cm.

## Edge Rate of Signal Determines T-Line Effects

### Backplane Details:

0.8" card spacing  
2 mm HM connectors  
100 Ohm diff. line  
 $R_T = 56 \text{ Ohm}$



### Differential TDT simulation vs signal edge rate

- 1.0 ns
- 0.5 ns
- 0.3 ns
- stub = 0.5"
- 11slot, DR@8, Sim@7
- (Ref. NESA WP)

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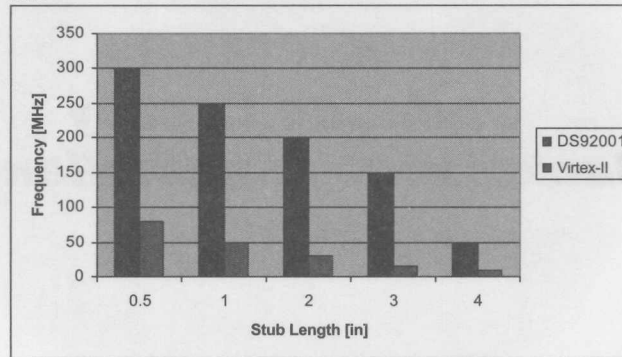
16

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In this simulation plot, we view the resulting waveshape as the Y axis is voltage, and the X axis is time. Note the resulting ring that is generated has the fastest transition time. Also note that the edge with 1 ns is very clean, however this may be too slow in many applications. As the signal travels down the interconnect, it will be further filtered (slowed). Thus,  $F_{MAX}$  needs to be checked at the furthest location, while ring should be checked at the first receiver load.

## **$F_{MAX}$ vs. Stub Length** **Small 7-Slot Backplane**

Higher  $F_{MAX}$  indicates better performance margins at lower data rates



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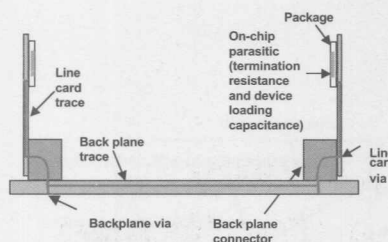
The following graph shows maximum frequency dependence on the stub length. The DS92001 is a robust “stub hider” which is optimized for backplane operation between 50-400 Mbps. This is the type of performance gain that can be achieved by careful placement of National LVDS devices close to the connector, where large FPGA packages cannot be routed efficiently. The optimized Bus LVDS I/O gives significantly improved performance even when the stub lengths are equal for both products, which is unlikely given the package size disparity. The performance data in this graph is based off of IBIS simulations of a theoretical 7-slot backplane with cards placed 25 cm apart.



## **Updating Legacy Backplanes is a Challenge**



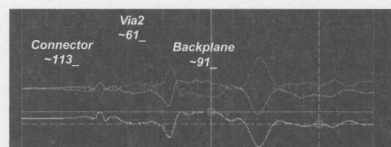
# High-Speed Backplane Challenges



*Backplanes are complex environments*

*At multi-gigabit speeds, design challenges at lower speeds become more difficult to manage*

*Channel issues: Crosstalk , ISI,  
Design issues: Connector and board*



TDR of Line Card into Backplane



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Backplane applications are complex and often have many impedance discontinuities in the data path. Careful design of a backplane with multiple components is critical to obtain good signal integrity.

Backplane design is a huge challenge. It deals with high frequencies, signal loss, and distortion coupled with legacy connectors and backplanes.

## High Speed Backplane Challenges

- Channel issues
  - Skin Effect
  - Crosstalk
  - Dielectric loss
  - ISI

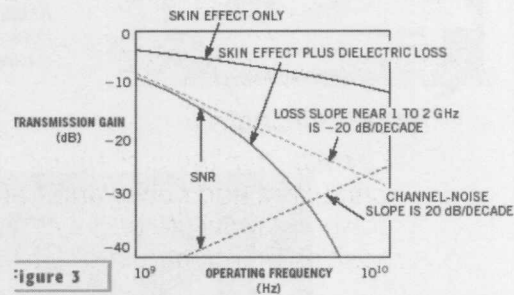


Figure 3

Amplitude Loss  
with Frequency

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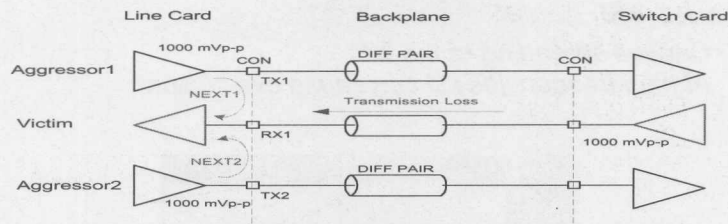
20

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One of the main issues in a channel is the frequency dependent loss of amplitude. Sources of major loss are Dielectric losses due to the substrate, skin effect due to the traces, and crosstalk from adjacent signals.

At multi-gigabit speed, these effects cannot be ignored.

## High-Speed Backplanes Challenges



- **Issue: Crosstalk**

- Results from the placement of high density connectors and backplane traces
- Lowers bandwidth of the channel, decreases receiver timing margin of the victim channel



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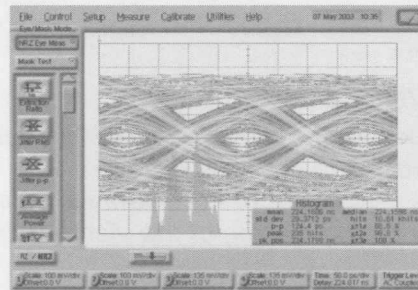


One of the reasons for signal degradation is crosstalk. Here we show the effect of NEXT or near end crosstalk which is the more dominant effect. The noise generated by crosstalk can decrease bandwidth and reduce receiver timing margins. This issue needs to be addressed by backplane interface devices.

*NEXT = Near End Cross Talk*

## High-Speed Backplane Challenges

- Issue: ISI
  - Causes spreading of the bits
  - At high frequencies ISI can cause eye closure



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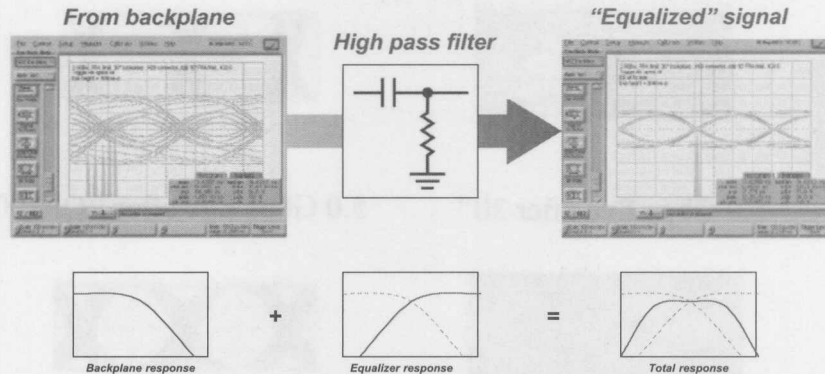


The frequency dependent loss results in an issue called Inter Symbol Interference or ISI. ISI causes the bits to spread or smear. For higher loss channels, ISI can be so bad that the eye is closed.

Inter-Symbol Interference (ISI), sometimes called data-dependent jitter, is usually the result of a bandwidth limitation problem in either the transmitter or physical media. With a reduction in transmitter or media bandwidth, limited rise and fall times of the signal will result in varying amplitudes of data bits dependent on not only repeating-bit lengths, but also dependent on preceding bit states. In addition, improper impedance termination and physical media discontinuities also will result in ISI due to reflections that cause signal distortions.

# Signal-Conditioning Techniques

## How Equalization Works



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RC filter used to show the effects of  
equalization on a backplane signal.

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What is equalization?

Backplanes and cables are bandwidth limited and act as low pass filters, filtering out high-frequency components of the signal. This creates ISI distortion as shown on the upper left.

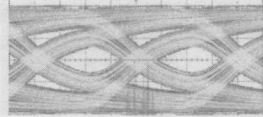
The receiver EQ is a high-pass filter which counteracts or "flattens" the backplane's frequency response. The signal that the receiver actually sees after equalization has a more balanced mix of low and high-frequency components, resulting in less jitter and a larger eye opening (upper right).

One can think of equalization in terms of a car radio's equalizer. The driver will adjust bass and treble controls (the equalizer) to compensate for the uneven frequency response of the car's speakers and interior (the backplane), resulting in a more faithful sound (the received signal).

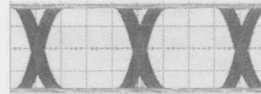
## Signal-Conditioning Techniques

### Fixed Equalizer (EQ50F100)

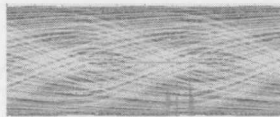
2.5 Gbps Eye after 30"



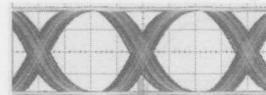
2.5 Gbps Eye after EQF100



5.0 Gbps Eye after 30"



5.0 Gbps Eye after EQF100



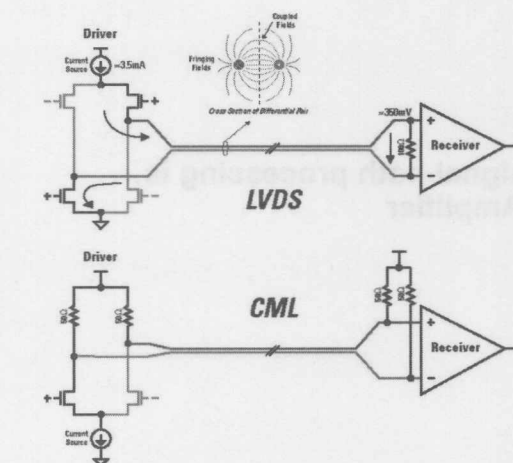
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These simulation shots show the "cleaning up" of the eye using equalization.

## LVDS vs CML



- LVDS is TIA/EIA-644-A standard

- No standard for CML

- LVDS operates in multiple configurations up to approximately 1 Gbps

- CML operates up to 10 Gbps but limited to point-to-point applications

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Providing higher bandwidth through applications without upgrades is a challenge. LVDS signaling is no longer capable of supporting bandwidth requirements above approximately 1.5 Gbps.

For really high speed data rates, CML is an option.

## ***Life at the Sharp End***

### **The start of the signal-path processing is... the Operational Amplifier**



26



Many signal paths start with that most universal of analog components, the operational amplifier\*. First named for its ability to perform mathematical operations (addition, subtraction, integration, differentiation etc) the modern Op-Amp provides the interface to many transducers and sensors, starting the process of converting real-world sensations such as sound, temperature, pressure, and light into electrical signals. Many signal sources simply require amplification or buffering, while others require manipulation to correct transducer or transmission errors. Op-Amps often can combine many of these functions, because the transfer characteristic of an Op-Amp is determined primarily by the external components connected around the Op-Amp.

Despite the fact that the Op-Amp is essentially a five-terminal device, with two input pins, two supply pins (or supply and ground), and one output pin, there are literally hundreds of Op-Amp types. National alone has more than 300 different types of Op-Amp, not counting duals, triples, and quads as separate types, and other manufacturers have similarly large portfolios.

During this seminar we will take a look at the characteristics that distinguish these Op-Amp types, why they are different, and how to choose the "right" Op-Amp. Techniques for solving common Op-Amp problems will be described, along with practical circuit applications.

The Op-Amp is only the first part of the signal path. Later on we will show how to accurately convert the signal to a digital format and then transfer that digital data, again without errors, to a storage or processing medium.

However, that is not where the signal path ends. Very often the signal information needs to be put back into a way that we in the "real world" can comprehend, either directly from the source or from the storage medium. Closing the circle, Op-Amps or their cousins are used to drive speakers, display devices, motors and RF transmitters.

\* A notable exception is RF receivers.

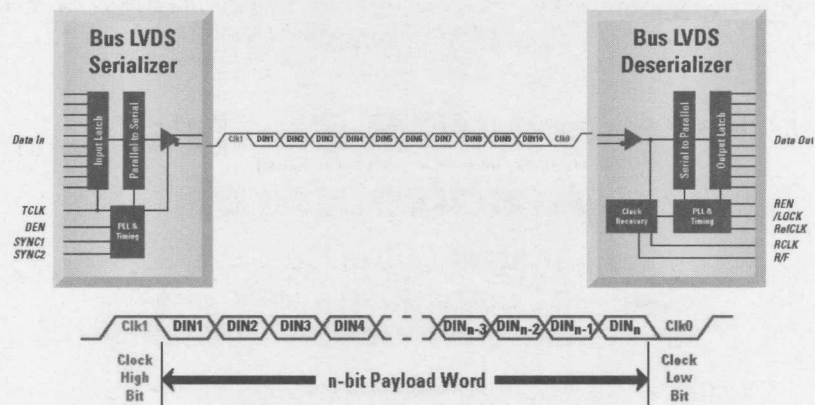




## ***Bus LVDS SerDes Architecture***

**Advantages of the Bus LVDS  
SerDes “Embedded Clock Bits”  
Architecture versus 8b/10b coding**

## Bus LVDS SerDes Operation



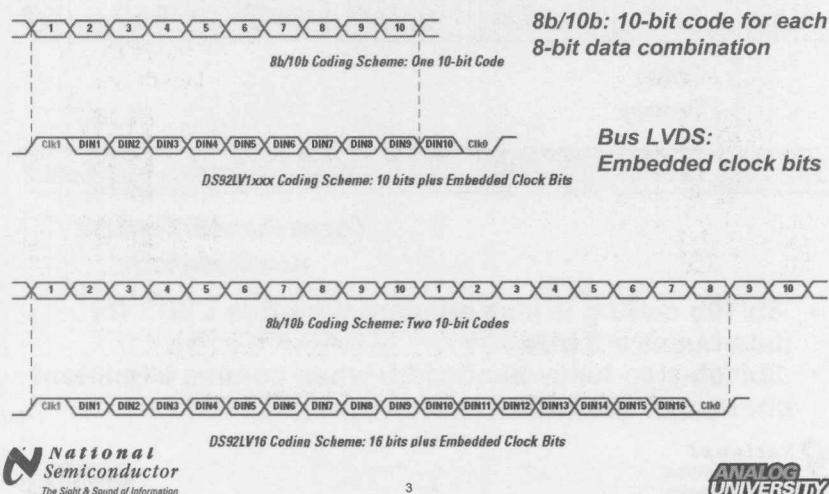
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The Bus LVDS SerDes devices serialize 10, 16, or 18 bits, embed the clock, and send this information across one pair. The clock is embedded as two bits, a high clock bit C1 and a low bit C0, which frame the data and provide precise timing information to the receiver. The receiver uses this timing information to recover the data.

## Coding Schemes Compared



3

Serial interconnects form the critical backbone of modern communications systems, and hence, the choice of Serializer/Deserializer (SerDes) can have a big impact on system cost and performance. While the maze of choices may seem confusing at first, SerDes devices fall into a few basic architectures, each tailored to specific application requirements. A basic understanding of these architectural differences enables the designer to quickly find the right SerDes for the application. In this presentation, we examine several distinct SerDes architectures and show how each plays a vital role in today's systems.

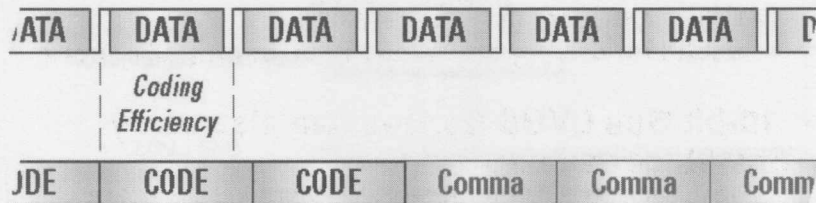
8b/10b-coding and embedded clock are two of the most popular coding schemes. Each has its strengths and weaknesses.

8b/10b-coding schemes guarantee multiple transitions as well as DC-balanced data. This is particularly good for byte-oriented data transmission in standards such as Ethernet, Fiber Channel, and Infiniband.

Embedded clock coding schemes do not guarantee DC-balanced data, but guarantee at least one low to high transition every clock cycle. This type of coding is well suited for non-byte oriented data such as applications requiring raw data plus control signals. Also, because embedded clock coding schemes do not lock to an external clock source, this relaxes jitter requirements for both the transmitter input clock and the receiver reference clock (only used before the receiver is locked to the incoming data stream).

Also, as shown in the slide, embedded clock coding schemes are not byte oriented, so word widths are not constrained to byte multiples. This increases payload efficiency as shown above.

## Efficiency



*Comma Character Overhead  
(Lost Bandwidth)*

- 8b/10b coding is less efficient than Bus LVDS for data buses > 8 bits
- 8b/10b also loses bandwidth when comma alignment characters are sent



4



The embedded clock bit architecture serializes the data bus and the clock onto one serial signal pair. Two clock bits, one low and one high, are embedded into the serial stream every cycle, framing the start and end of each serialized word (hence the alternative name "start-stop bit" SerDes) and creating a periodic rising edge in the serial stream. Data payload word widths are not constrained to byte multiples; 10- and 18-bit widths are popular bus widths.

The 8-bit/10-bit (8b/10b) serializer maps each parallel data byte to a 10-bit code and serializes the 10-bit code onto a serial pair. The 10-bit transmission codes were developed by IBM Corporation in the early 1980's and guarantee both multiple-edge transitions every cycle as well as DC balance (balanced number of transmitted ones and zeros). Frequent edge transitions in the stream allow the receiver to synchronize to the incoming data stream. DC balance facilitates driving AC-coupled loads, long cables, and optical modules.

As also mentioned in the previous slide, embedded clock coding schemes are not byte oriented. Therefore, 8b/10b coding is not efficient for data buses >8 bits. Also during the receiver synchronization period, comma characters must be sent for the receiver to lock. Efficiency is further decreased during this process.

## **DC Balance Coding**

**Using Bus LVDS SerDes with 8b/10b-Coded Data**

- **8b/10b coding is DC balanced**
  - useful for driving optical modules or long distances
- **10-bit Bus LVDS SerDes can also carry 8b/10b coded data**
  - you get both DC balance AND Bus LVDS SerDes benefits

*DS92LV1021/1212A Carrying 8b/10b Payload*



5



National's Bus LVDS SerDes does not restrict the type of data that can be transmitted. Therefore, 8b/10b coding also can be transmitted for optimum performance in optical modules or long-distance cable applications.

## **Start-Stop vs 8b/10b Coding**

### **Overview**

Parameter	8b/10b	Start-stop
Latency	Medium	Low
Lock to random data	Need to add commas	Yes
Data bus width	Byte-oriented	Flexible
Transmit clock jitter tolerance (RMS)	5-10 ps	80 or 120 ps
Reference clock tolerance	$\pm 0.01\%$	$\pm 5\%$
DC balanced coding	Yes	Need to add scrambling
Number of vendors	Many	Several

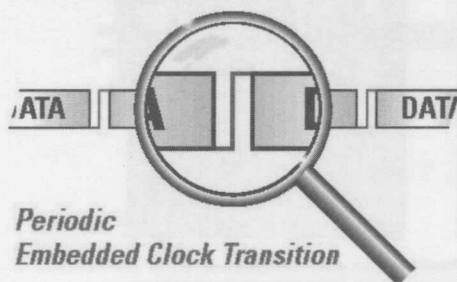


6



Both embedded clock bit start-stop and 8b/10b coding SerDes architectures are common in 3G basestations and each architecture has distinct advantages. The choice of SerDes technology ultimately depends on the goals and priorities of the application.

## Embedded Clock Edge



- Embedded clock bits give precise timing information to the receiver every cycle
- Benefits
  - Relaxed input clocking requirements
  - Lock to random data capability
  - Flexible bus widths

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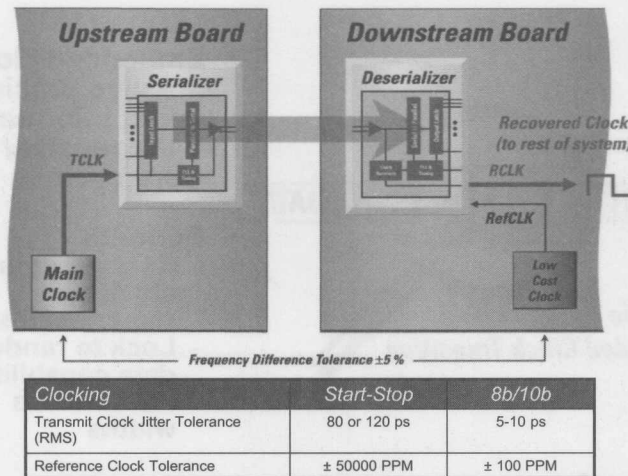
All Bus LVDS SerDes chips employ an embedded clock bit architecture in which the embedded C0 and C1 clock bits create a clock edge every data cycle. This precise and regular timing signal gives the following unique advantages:

- The periodic timing information means the receiver does not need to rely on a local reference clock for precise timing. Since the local reference clock need only be within  $\pm 5\%$  of the transmit clock frequency (versus  $\pm 100$  PPM for most SerDes), an inexpensive local clock source may be used.
- Since the C0/C1 bits frame each data payload, the receiver can lock to random data. True live insertion is achieved and no bandwidth-robbing training patterns are needed.
- Not tied to a fixed scrambling scheme, Bus LVDS SerDes can be designed to handle non-byte-oriented payloads. For example, the 10-bit Bus LVDS SerDes carries a full 10-bit payload. These 10 bits can be used for any kind of info such as: data bits, frame bits, parity, etc.



## Relaxed Clocking Requirements

### Using Only One Precision System Clock



8

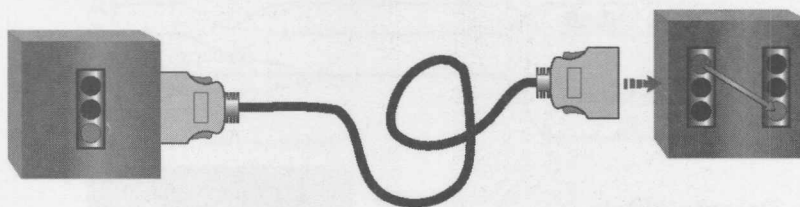
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**UNIVERSITY**

As mentioned previously, the Bus LVDS's relaxed clocking requirements allow customers to use low-cost clocks.



## **Lock to Random Data**

### **One Receiver**



- **No feedback path required from receiver to transmitter to initiate training pattern**
  - “Plug & go”
  - No training patterns required!

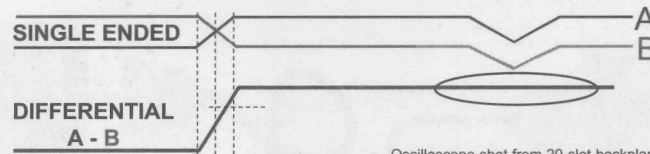


9



Bus LVDS SerDes have power-up high impedance and lock to random data for true “plug & go” live insertion. Lock status feedback and training patterns are not required.

## Bus LVDS Supports Hot Insertion

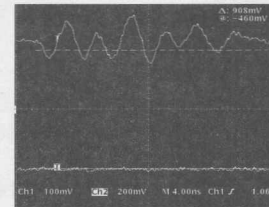


- Rejects glitch resulting from backplane card insertion

100mV glitch on signal A

No Glitch on differential signal

Oscilloscope shot from 20-slot backplane



Backplane probed with single-ended and differential probes

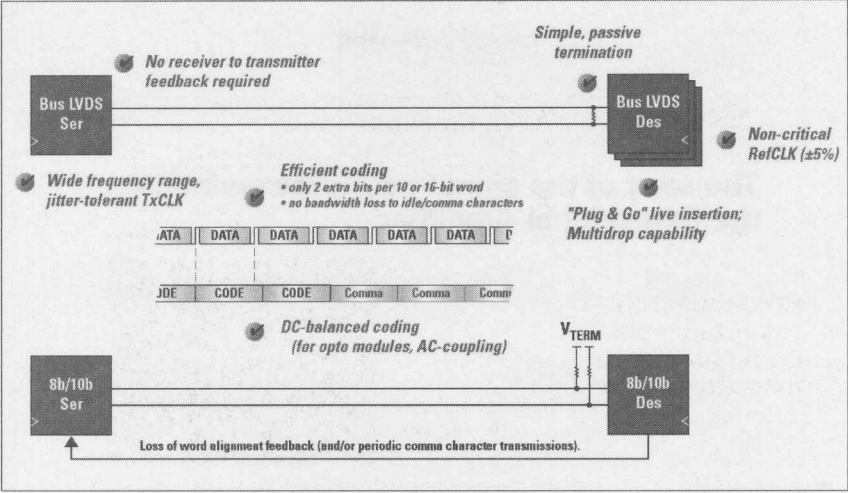
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When a Bus LVDS receiver or other device is inserted onto a backplane, the capacitance it adds creates a common-mode glitch. However, since National's Bus LVDS receivers reject common-mode noise, data is not impacted.

## Bus LVDS Summary



Bus LVDS SerDes are very flexible and efficient parts. They do not require special training patterns to lock, have simple termination techniques, have relaxed timing requirements, support hot-insertion, do not restrict the type of data sent to the transmitter, and have very efficient coding that practically eliminates interconnect bandwidth loss due to idle or comma characters.

## ***Life at the Sharp End***

### **The start of the signal-path processing is... the Operational Amplifier**



12



Many signal paths start with that most universal of analog components, the operational amplifier\*. First named for its ability to perform mathematical operations (addition, subtraction, integration, differentiation etc) the modern Op-Amp provides the interface to many transducers and sensors, starting the process of converting real-world sensations such as sound, temperature, pressure, and light into electrical signals. Many signal sources simply require amplification or buffering, while others require manipulation to correct transducer or transmission errors. Op-Amps often can combine many of these functions, because the transfer characteristic of an Op-Amp is determined primarily by the external components connected around the Op-Amp.

Despite the fact that the Op-Amp is essentially a five-terminal device, with two input pins, two supply pins (or supply and ground), and one output pin, there are literally hundreds of Op-Amp types. National alone has more than 300 different types of Op-Amp, not counting duals, triples, and quads as separate types, and other manufacturers have similarly large portfolios.

During this seminar we will take a look at the characteristics that distinguish these Op-Amp types, why they are different, and how to choose the "right" Op-Amp. Techniques for solving common Op-Amp problems will be described, along with practical circuit applications.

The Op-Amp is only the first part of the signal path. Later on we will show how to accurately convert the signal to a digital format and then transfer that digital data, again without errors, to a storage or processing medium.

However, that is not where the signal path ends. Very often the signal information needs to be put back into a way that we in the "real world" can comprehend, either directly from the source or from the storage medium. Closing the circle, Op-Amps or their cousins are used to drive speakers, display devices, motors and RF transmitters.

\* A notable exception is RF receivers.



## ***Typical Applications***

The next section shows some typical applications where LVDS is used.

## ***High-Speed Interface in Multiple Markets***

- **Telecom:** Access and transmission equipment
- **Datacom:** Routers, switches, access
- **Imaging:** Copiers, printers, scanners, cameras
- **Medical:** Imaging and sensor interconnect
- **Industrial:** Backplanes, cameras, graphical flat panels, robotics, control systems, sensor interconnects
- **Consumer:** DVD R/W, sensor interconnects, flat panels for notebooks, all-in-1s, desktops, workstations, wearable displays

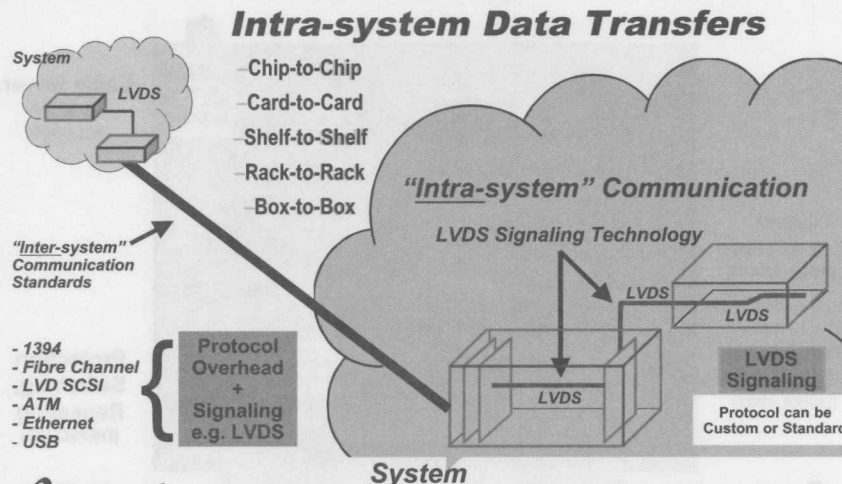


2



LVDS addresses a generic need that spans many market segments. Data-intensive applications are the common denominator here. This slide lists some of the many LVDS possibilities including telecom, datacom, imaging, industrial, medical and PC applications.

# When and Where to Use LVDS Interface



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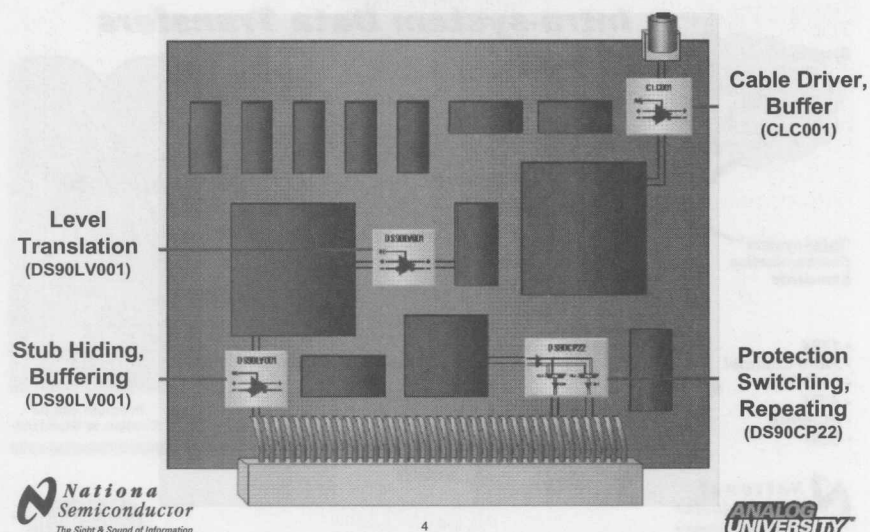
LVDS is just an electrical signaling technology used to convey 1s and 0s. Since high-speed information needs to move into and throughout a system, there is a need to communicate this information to the outside world – inter-system – through an agreed upon protocol standard. This is what IEEE 1394, Fiber Channel, Gigabit Ethernet, etc. are used for today.

However, this information also needs to move THROUGH (i.e. within) a system and this is where National's LVDS solutions are used today. Since the hardware and software overhead associated with the protocol solutions listed above are not needed (and would be redundant and expensive) a simple, low-cost LVDS link is used. Thus, National's LVDS solutions move information intra-system: on a board, board-to-board, module-to-module, or box-to-box. In the future, however, LVDS will be used with protocols for inter-system communication too.

Note: The standards 1394, SCI, and LVD SCSI actually use signaling technologies similar to and/or derived from LVDS and combine this with protocols to create an intersystem communication standard.



## **Buffer, Cable Driver, Level Translator Applications**



Some advanced ASICs and FPGAs include LVDS I/O options. Sometimes the design of these LVDS cells does not take full account of the analog nature of high-speed signaling. Operating at megabits or gigabits per second requires fast edge rates and precise circuit timing. At these speeds, the bus or cable to be driven is modelled as a transmission line - not a lumped load. Driving off the printed circuit board (PCB) with these digital LVDS I/Os may result in poor signal quality, requiring an LVDS-to-LVDS buffer to "boost" the signal. The DS90LV001 is an 800 Mbps single LVDS/LVPECL to LVDS buffer and is available in a 3 x 3 mm package. Its small size allows it to be added to dense PCBs to improve signal integrity without a major re-layout of the PCB, making it a useful last-minute fix.

Many older high-speed ASICs and standard devices use LVPECL signaling. LVPECL I/Os have great signaling characteristics, but are not compatible with today's CMOS circuits. Therefore, a system design may be a mix of older Bipolar/BiCMOS LVPECL and newer CMOS LVDS devices, resulting in the need to translate between LVPECL and LVDS. For translating from LVPECL to LVDS, the DS90LV001 and the DS90CP22 800 Mbps/Channel 2x2 switch directly accept LVPECL signals, providing a clean LVDS output. Just directly connect your LVPECL output to the DS90LV001 or DS90CP22 input. For LVDS to LVPECL translation and translation to/from PECL, a passive resistor network is needed to adjust voltage swing and/or bias (there are numerous application notes on this from various PECL vendors).

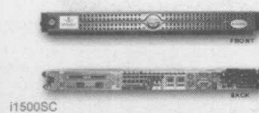
The DS90LV001 and CLC001 can be used to translate between LVDS, LVPECL, and PECL. The DS92001 (not shown) can be used to convert from LVDS or LVPECL to Bus LVDS. The CLC001 has a very wide input common-mode range and can accept both LVDS and LVPECL inputs.



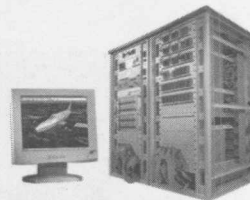
## Typical Applications



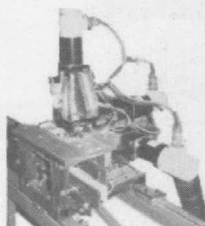
Industrial Control &  
Automation



Storage Area Networks



Test Equipment  
(Simulator)



Scoreboards



Industrial CCD Cameras



5



SerDes parts will fit into a wide variety of applications. Basically any place where large amounts of data must be transmitted over distances of less than 30 meters very cleanly at low power with less cable or anytime when 30 MHz or greater clock distribution is needed. Examples of applications could be printers where data is sent from the front end to the print head, an industrial printer that is used to print large images on billboards, or scoreboard displays such as in the middle of a sports arena.

Printers

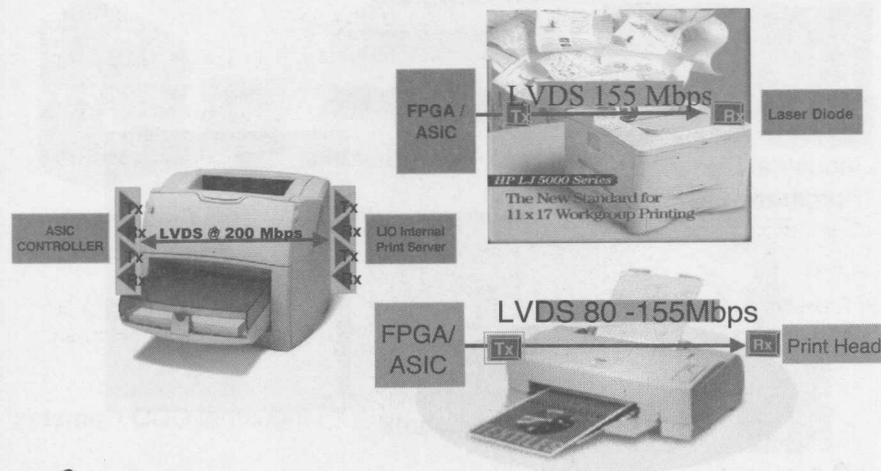
Copiers

Storage Area Networks

Industrial

## Typical Applications

### Printers and Copiers



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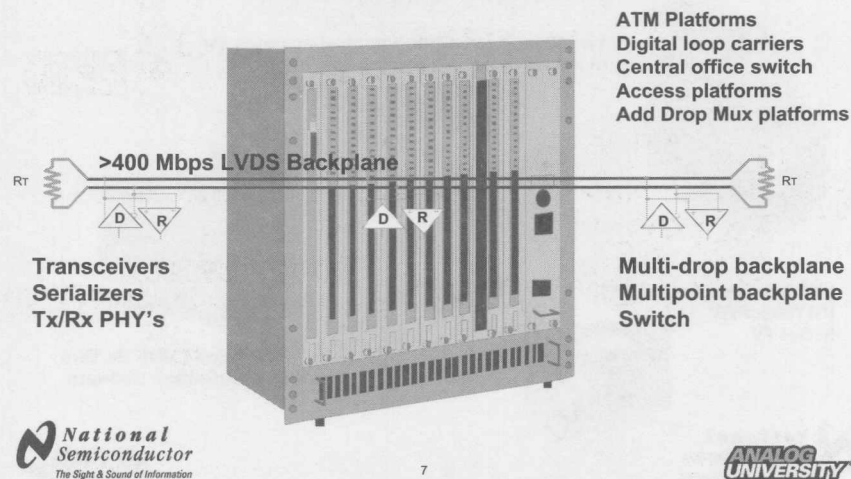
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LVDS is the technology of choice for medium-speed, low-power, robust communication to sensitive high-performance analog printer components.

LVDS data rates are well suited for most print applications where data from an ASIC or FPGA in a printer is transmitted to a print head or laser diode.

## Typical Applications

### Telecom/Wireless

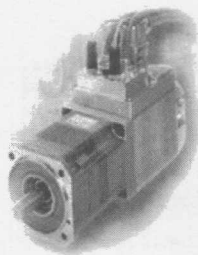


BLVDS (Bus LVDS) extends LVDS benefits into heavily loaded backplane applications. It also has several enhancements for multipoint (multiple driver) applications as noted above. Note that these are a collection of optimized parts (not a family of identical I/O). Therefore, a careful review of the part's datasheet is recommended to ensure proper usage.

BLVDS also services other backplane-optimized applications such as limited multi-drop and point-to-point links. Noting that the bus is multi-driver, BLVDS (and M-LVDS) drivers tend to support high-impedance bus pins when powered-off, and also glitch free power up/down. These are useful when adding nodes to an active shared bus.

Many telecom and wireless applications require multi-drop or multipoint configurations. National's Bus LVDS family of devices are well suited for these type of applications. Please visit us at [lvds.national.com](http://lvds.national.com) for the world's largest selection of interface devices.

## Typical Applications

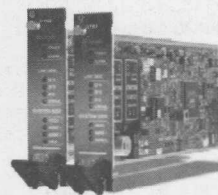


10/100 PHYs in motion control systems for machine tools and production machines

LVDS SerDes and 10/100  
PHY/MacPHY  
In flat TV



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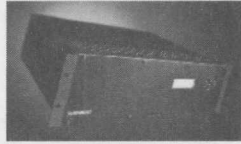
Integrated LVDS SerDes  
in video distribution Network

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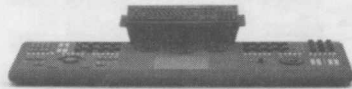
8

National Semiconductor has a large selection of products ranging from 10/100 PHYs in the industrial market to LVDS wideband SerDes in the video market to a combination of both in the consumer markets.

## Typical Applications



HD/SD broadcast video chipset and Gigabit Ethernet Copper PHY in video decoder/distribution switch and film studio postproduction color correction



HD/SD-SDI chipset in broadcast video server



Networked Servers for Hi-Def Production



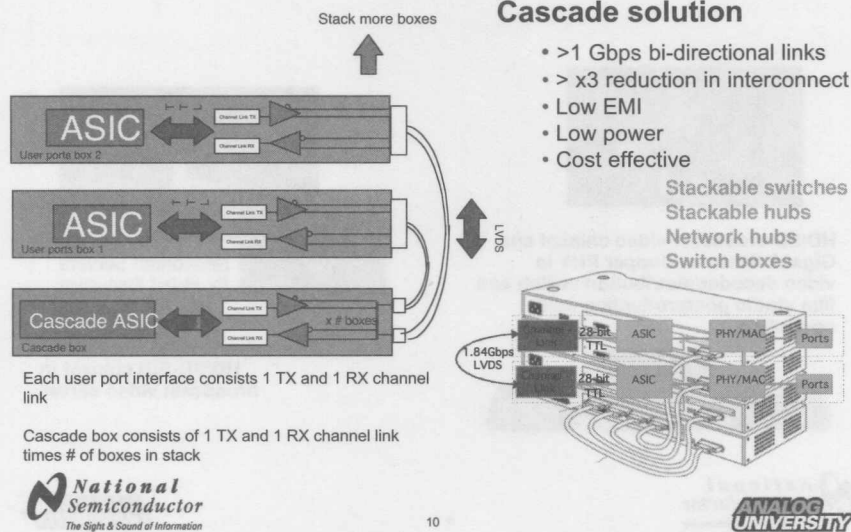
9



Among National Semiconductor's interface product folders is a family of broadcast video products. The broadcast video family of products covers a wide range of applications, some of which include the broadcast video server market.

## Typical Applications

### 24-port 10/100 Stackable Ethernet Switch

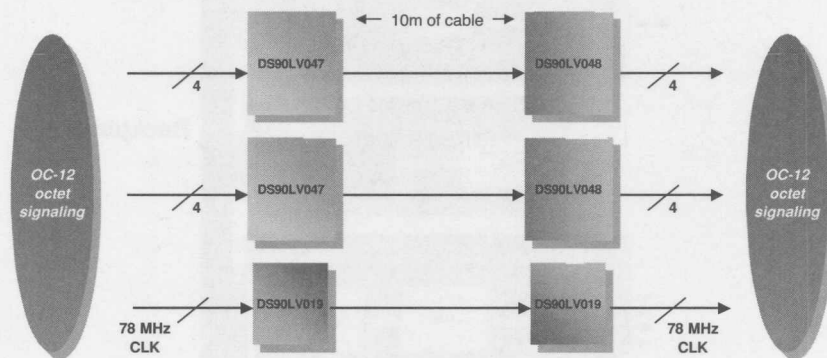


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Here is a stackable switch. The Ethernet ports are on the front, and the LVDS interface is up the back of the box. There is a separate up and down link per box with the main switch on the bottom. This allows for full-duplex transmission and a non-blocking architecture.

## Typical Applications

### Point-to-Point transport of OC-12 (622 Mbps) payload



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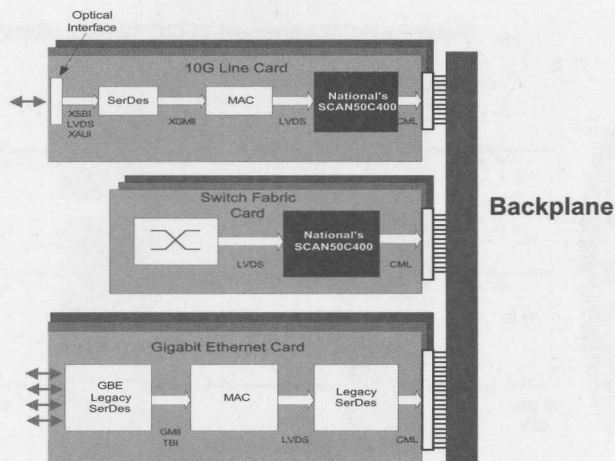
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This example shows how OC-12 or STS-12 can be transmitted over cable lengths up to 10-15 meters using basic LVDS physical layer devices. The high-speed 622 Mbps signal is broken down into a lower-speed 8 differential pair parallel interface. Multiple chips can be used in parallel to accomplish this as shown above, as long as timing margins are not violated. This allows ASIC or FPGA devices to easily handle the data stream.

STS-12 is electrical version of OC-12



## Typical Applications



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National's SCAN50C400 SerDes is ideal for increasing throughput on existing FR-4 backplanes.

The SCAN50C400 is a four-channel high-speed backplane transceiver (SerDes) designed to support multiple line data rates at 1.25, 2.5, or 5.0 Gbps over a printed circuit board backplane. It provides a data link of up to 20 Gbps total throughput in each direction (40 Gbps in full duplex applications).

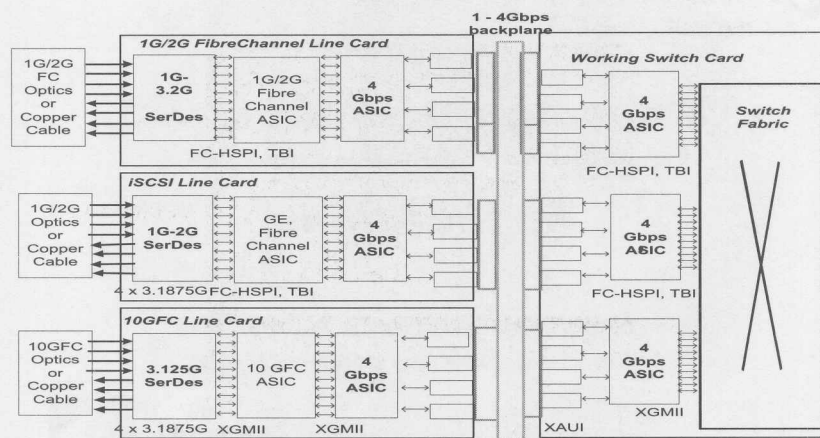
Each transmit section of the SCAN50C400 takes a 4-bit differential LVDS source synchronous data bus, serializing it to a differential high-speed serial bit stream that is output from a CML driver. The receive section of the SCAN50C400 consists of a differential input stage, a clock/data recovery PLL, a serial-to-parallel converter, and a LVDS output bus.

De-emphasis at the high-speed driver outputs and a limiting amplifier circuit at the receiver inputs are used to reduce ISI distortions to enable error-free data transmission over more than 26 inches point-to-point link with a low-cost FR4 backplane. Internal low-jitter PLLs are used to derive the high-speed serial clock from a differential reference clock source. Two channels share common transmit and receive LVDS clocks.

The SCAN50C400 also has built-in self-test (BIST) circuitry and loop-back test modes to support at-speed self-testing.



## Fiber Channel Application EQ50F100 Equalizer



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The EQ50F100 is a 6.25 Gbps equalizer designed to compensate transmission medium losses and reduce the medium-induced deterministic jitter. It is optimized for printed circuit backplanes for up to 30" of FR4 with backplane connectors at both ends. It is code independent and functions equally well for short run length balanced codes such as 8b/10b. It also is commonly used in multiplexed 1.25 Gbps Ethernet Systems.

The equalizer uses differential CML inputs and outputs with feed-through pin-outs, mounted in a 3 mm x 3 mm 6-pin leadless LLP<sup>®</sup> package.



## **Choosing the Right LVDS Products for Interface Applications**

**"Processing power is NOTHING  
if the data has no place to go"**



The next section discusses specific applications and how National parts can be used to solve these application problems.

*The Analog Edge*  
*AN → > 100 mtr*  
*LVDS*

## ***Application Example***

1. Sketch an option to realize a cable interface (up to 10 m) from a CCD inspection camera (24-color bits + 4 control signals, clocked at 66 MHz) to a frame-grabber image processing card.

2. Chipset must operate --40 to 85C temp range



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**ATmel AVI/VA C2 CL 4010**

**Matrox Meteor-II/ Camera Link (METEOR2-CL/32)**

VIDEO →  
LVAL →  
DVAL →  
CLK →  
EXP1 (CC1) ←

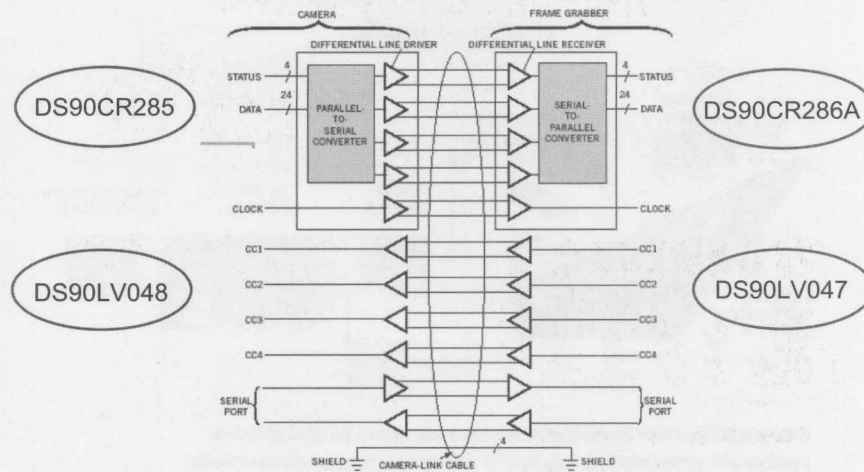


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13-16

## Machine-Vision Application



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The Camera Link standard rationalises the camera-to-frame-grabber connection but still allows latitude for dedicated I/O signals and future growth.

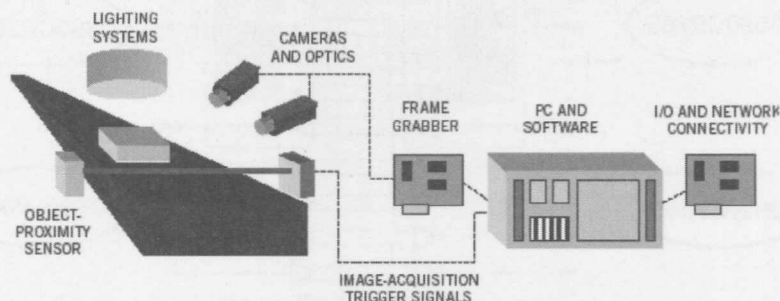
17

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By combining LVDS physical layer devices with Channel-Link SerDes, the Camera Link specification is able to specify an economical cable and achieve very high overall throughput. This enables clear, sharp image information to be displayed from remote camera locations.

As shown above, for additional channels to the monitor, multi-channel LVDS drivers such as the DS90LV047/ DS90LV048 may be used.

## Machine-Vision Application



A basic machine-vision application comprises a camera and its lighting system together with communication links to a PC that runs the image-analysis software.



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Embedded clock bit SerDes are especially well suited to applications that transmit raw data plus other signals such as control, parity, frame, status, etc. Examples include signal-processing systems such as base stations, automotive imaging/video, and sensor systems where an analog-to-digital converter, camera, or display communicates raw data with the processing unit at the other end of the link. To illustrate, suppose National Semiconductor's DS92LV18 is used in the data acquisition. The DS92LV18 serializes not only the data, but also two extra bits of additional information such as parity, status, etc. These bits are serialized along with the data at the normal A/D sampling rate so no data buffering or extra logic is required.

Using an 8b/10b SerDes in the same application would be more complicated. The extra non-byte-oriented control information must be buffered and sent in byte format. A K28.5 comma character also must be sent at the start of link synchronization, requiring additional logic. These extra "non-data" bytes require the SerDes to operate faster than the data conversion rate. This not only places higher demands on backplane or cable design, but also requires some kind of idle insertion/deletion flow-control mechanism. While in data communications systems such buffering typically already exists, in many non-datacom applications this extra data processing adds unnecessary overhead and complexity. This example shows how a couple extra bits can make a big difference to the system design.

### Relaxed Clocking Requirements

Most SerDes depend on the tight jitter control of both the serializer transmit clock and a receiver reference clock to achieve and monitor lock. The embedded clock bit receiver, on the other hand, synchronizes to the incoming embedded clock rising edge and requires the receiver reference clock only during initial synchronization to prevent lock to a false harmonic. This relaxes the jitter requirement on both transmit and reference clocks by at least an order of magnitude. In fact, the reference clock need only be within  $\pm 50,000$  PPM of the transmit clock frequency. This can be a big cost saver in systems using non-standard oscillator frequencies since a very low-cost, standard frequency can be used.

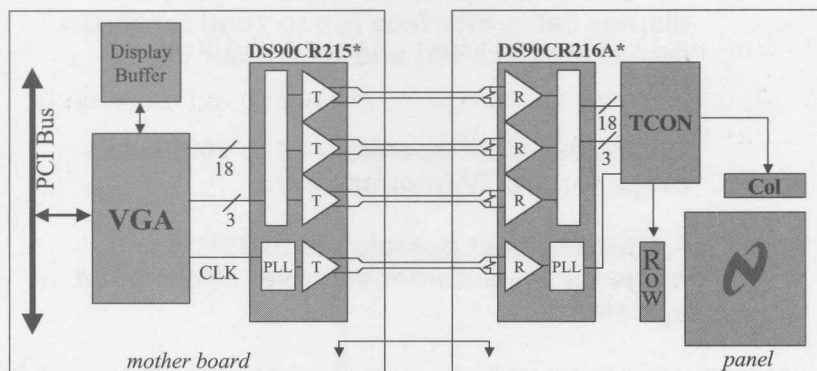
## ***Application Example***

1. Sketch an option to realize a flat panel display cable interface (up to 10m) for SVGA resolution (40 MHz) and 6-bit color depth RGB.
2. Chipset must operate  $-10$  to  $70^{\circ}\text{C}$  temp range for the TV interface card
3. Chipset must operate  $-40$  to  $85^{\circ}\text{C}$  temp range for the automotive driver information system



# Flat-Panel Display Applications

**Embedded displays in POS, coffee machines,  
driver-information displays etc.**



\*DS90C363 & DS90CF364 combination, if -10 to 70°C temp range suffices



20



One of the earliest adopters of Channel Link devices was and still is the notebook computer industry. These devices take the information from the host computer, serialize, and retransmit the information to the integrated display module. Using LVDS technology allows for a low-cost, low-noise, highly reliable interconnect to be established across the "hinge" of the notebook computer.

The Channel Link family of products is well suited for a variety of video type applications – some requiring more data bits, some requiring less. Many point-of-sale applications and even simple machines such as coffee machines can use Channel Link products.



## ***Application Example***

- 1. Uni-directional 32-bit bus (clocked @ 100 MHz)**
- 2. Data needs to be transferred between two processor cards through a back panel**



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## ***Life at the Sharp End***

### **The start of the signal-path processing is... the Operational Amplifier**



22



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\* A notable exception is RF receivers.



## **System-Level Troubleshooting**

## ***What Information Will You Be Asked For?***

- Find out the essential information:
  1. What driver/receiver is being used?
  2. What is the clock speed?
  3. What is the configuration?
  4. What are the operating conditions?
  5. How many connectors? What type?
  6. What cable is used? How long is it?
  7. What is the exact problem?
  8. When does the problem occur?
  9. Is the problem repeatable?
  10. Do you have a schematic we can look at?  
(Schematic Review Service in FY2005)



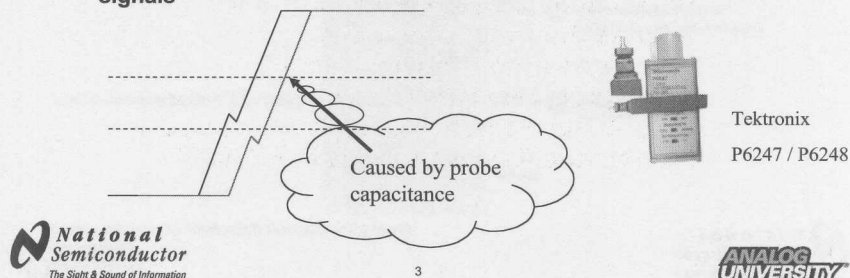
2



Always collect as much detailed information about the problem before contacting National. This will help you and our applications staff to consider all possible solutions and sources of the problem. Soon we will be providing a schematic review service on our web site where you can submit your schematics for review. Please check in the "What's New" section on our LVDS web page to see when this will be available.

## Looking at the High-Speed Signal

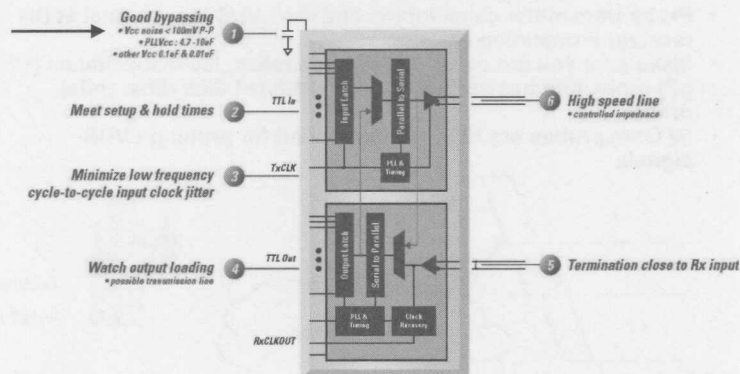
- Troubleshooting begins with looking at signals correctly along the interconnect path
- Probe transmitter clock inputs and the LVDS input signal at the receiver termination resistor
- Make sure you are using a high-impedance, low-capacitance ( $<1$  pF) probe that has sufficient bandwidth ( $>1$  GHz differential probes)
- 50 Ohm probes are NOT recommended for probing LVDS signals



System problems are often observed on the receiver side. Either the receiver does not lock, locks intermittently, or provides incorrect data. The best place to start troubleshooting is to look at the high-speed signals coming from the transmitter and directly at the termination resistor of the receiver. Always use high-impedance, low-capacitance probes with adequate bandwidth for the signal you are measuring.

## Check for Sources of Jitter – Bypass Capacitors

- What does the signal at the termination resistor look like?
  - Is there excessive jitter? Check  $T_{CLK}$  jitter and bypass circuitry.



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More info: Consult datasheet of chosen product

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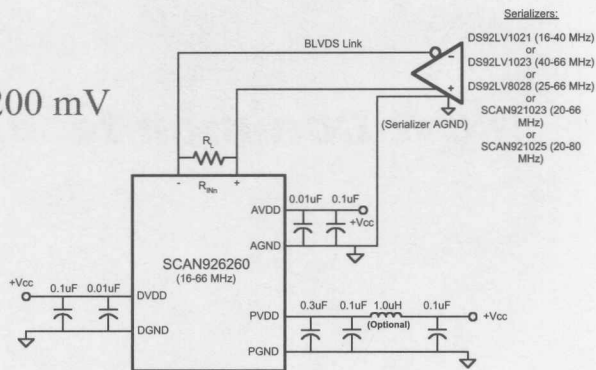
4

One of the most common problems found at the system level is noise. For most serial links, the noise can enter through the clock source or from the power supply pins. It's always good engineering practice to probe the clock source and power supply pins for excessive noise. Always try to keep noise on power supply pins to <100 mV p-p.

## Check for Sources of Jitter

- Does the application have adequate bypassing?

$$\Delta V_{DD} < 200 \text{ mV}$$



5



This is a typical bypass scheme pulled from the SCAN926260 datasheet. One important note is that any difference between the power pins should be less than 200 mV. Due to the design of ESD structures, a voltage difference greater than 200 mV can cause excessive jitter or in some cases latch up and damage to parts.



## ***Most Common Issues***

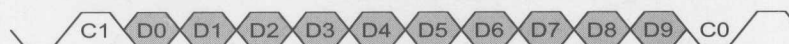
AN 1194  
Fail Safe  $\rightarrow$  Resistor



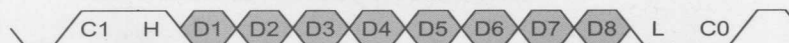
## The Receiver Doesn't Ever Lock – Embedded Clock Parts

- What is the pattern being sent upon power-up?
  - Is it an RMT Pattern?

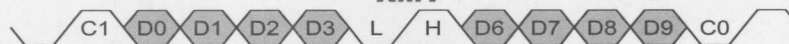
### Full 10-bit Payload



### 8-bit Payload



### RMT



### SYNC



7



A repetitive multi-transition (RMT) pattern is defined as a data pattern containing more than one fixed low-to-high transition in one clock cycle.

Sometimes you will find that a receiver never locks upon power-up. One of the most common reasons a receiver does not lock upon power-up is caused by the RMT pattern. If you must send RMT patterns upon power-up, SYNC patterns must first be sent from the transmitter. After the receiver locks to the SYNC pattern, you can send RMT patterns or any other type of data.

## The Receiver Provides Outputs When No Data is Being Sent

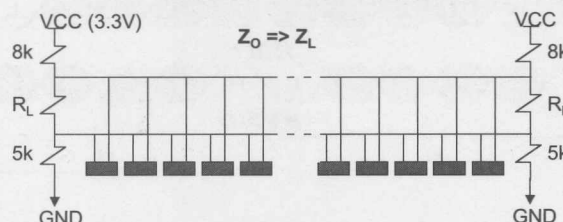
- Is the interconnect connected?

No:

- Add failsafe (see next slide)
- Powerdown the receiver (use PWRDN\* pin)

Yes:

- How are the LVDS lines laid out?
- Are there TTL signals routed near by?
- What is the routing through connectors like?



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See AN-1194 for detail and calculations for resistor values

8

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Failsafe biasing may be required if a known state is required on the bus when any of the following conditions occur:

- All drivers are in TRI-STATE® mode
- Drivers removed or powered-off

If this is the case, additional biasing (beyond the internal failsafe biasing of the receivers) may be provided with a power termination as shown above

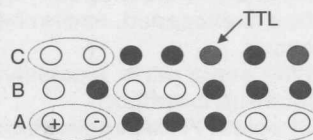
In selecting failsafe resistor values, note the following:

- Magnitude of the resistors should be 1 to 2 orders higher than the termination resistor to prevent excessive loading to the driver and waveform distortion
- The mid-point of the failsafe bias should be close to the offset voltage of the driver (+1.25V) to prevent a large common-mode shift from occurring between active and TRI-STATE (passive) bus conditions
- The pull-up and pull-down resistors should be used at both ends of the bus for quickest response
- Note that signal quality is reduced as compared to active driving (on/on)
- See AN-1194 for details and calculations

AN 1194

## The Receiver Loses Lock

- Is crosstalk an issue?
  - What does the signal at the termination resistor look like?
  - Are the LVDS lines closely coupled (reference LVDS Owner's Manual)?
  - How are signals routed through the connectors?
  - Place adjacent LVDS signals at least 2S away
  - Place TTL signals at least 3S away or route on another layer
- Crosstalk is very difficult to fix post layout



9



Connectors are a complex topic and are the subject of many wars at standards committee meetings. There are two basic types: standard matrix-based connectors (3 rows of 32 pins) and special connectors. The special connectors have elaborate techniques to clamp to the PCB and are stealth-like to a TDR! They are also very application specific and tend to be rather expensive. More common is the use of standard connectors for a mix of differential, power, ground, and single-ended connections. The above slide shows a typical pin-out recommendation for a combination of single-ended and differential signals. For differential lines in a matrix connector, adjacent pins within a single row results in the best signal integrity. Also, the row with the shorter path provides a better path over the longer row. Ground signal assignment should always be used to isolate large-swing (TTL) signals from the small-swing lines as shown in the example above.

Note that the noise issues caused by crosstalk are very difficult to fix after boards have already been laid out and fabricated. For this reason, all high speed board layout designs should be followed very closely. Many of these fundamental techniques are described in the LVDS Owner's Manual which can be downloaded free at [lvds.national.com](http://lvds.national.com).

## ***Jitter Content is High on My Transmitter Output(s)***

- Do you have a scope shot of the transmitter clock input?
  - How much jitter is on the transmitter clock input?
- How much noise is on the power pins?
  - As a general rule of thumb, VDD noise should always be under 100 mV
  - Add bypass capacitors to help filter noise
- How much over and undershoot is there?
  - Most datasheets specify 0.8V MAX of over/undershoot. When this is exceeded, excessive jitter at the LVDS outputs can occur.
  - With some parts, excessive over or undershoot causes a latch-up condition
  - Simplest FPGA application solution: see if output drive current on the FPGA can be reduced.



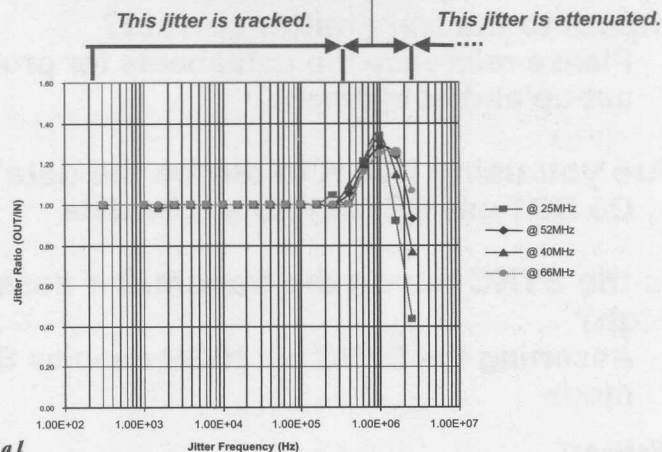
10



In addition to noise, a frequent problem is using FPGAs to over or under drive the TTL input pins. Excessive over or undershoot can cause excessive jitter on the high-speed outputs and has in some instances, caused a latch-up condition. Many FPGAs from Xilinx and Altera Corporation have outputs with configurable drive current. One simple solution is to reduce this drive current. Another alternative is to load the outputs with capacitors.

## Jitter Content is High on My Transmitter Output(s)

Attenuate the TxCLK and power supply noise in this range!



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Due to the design of our transmitter PLLs, jitter from approximately 800 kHz to 1.3 MHz should be attenuated. In this range, jitter will be amplified and can cause system performance issues.

## **Data Recovered from the Receiver is Incorrect**

*"I get wrong data all the time."*

- Are the set-up and hold times for the data inputs to the transmitter correct?
  - Please reference the datasheets for proper set-up and hold times
- Are you using RCLK to strobe the data?
  - Do NOT use REFCLK to strobe data
- Is the SYNC pin on the transmitter asserted high?
  - Asserting the SYNC pin HIGH enables SYNC mode



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These are some of the most common reasons data recovered from the receiver may be incorrect. Always verify that the set-up and hold times on the transmit side are being met. In addition, always make sure you are using RCLK to strobe output data. **RCLK is an output** used to strobe data, and **REFCLK is an input** used by the PLL for reference.

## ***Do I Need To Use REFCLK?***

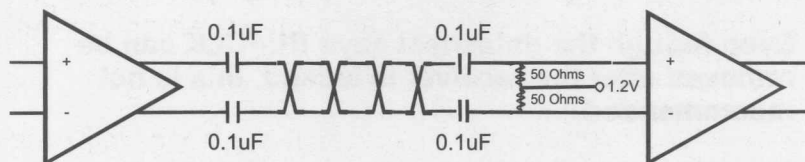
- YES
- The reference clock is used to strobe the incoming data whenever the receiver is unlocked
- Even though the datasheet says REFCLK can be removed after the receiver is locked, this is not recommended
- There is NO phase relation between REFCLK and RCLK
- There is also no phase relation between REFCLK and TCLK



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## What Is The Proper Termination for AC Coupling?



NOTE: Assumes a 100-Ohm termination resistor



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AC-coupling LVDS signals removes the 1.2V common-mode voltage. Two 50 Ohm to GND series resistors with a center tap to 1.2V can be used to restore the common-mode voltage. There are also AC coupling experiment reports available from National. Please contact us for more information on optimizing AC-coupled applications.



## ***Sometimes a Specific Data Pattern Causes the Receiver to Lose Lock – AC Coupled***

- Sometimes, 0.1uF is not the correct capacitor value to use
- If the clock speed is slower (20 MHz) and a SYNC type pattern is sent, there are not enough transitions in the data pattern
- The lack of transitions causes the AC coupling capacitors to filter out the signal
- Use a larger AC coupling capacitor, e.g. changing from a 0.1uF to 1uF capacitor
- With all AC-coupled applications, the smallest available package should be used. This reduces the amount of package parasitics that may affect signal integrity



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For parts that do not provide encoded data (such as 8b/10b coding), there may not be enough transitions in the pattern for standard 0.1uF capacitors. A larger capacitor can sometimes solve signal integrity issues. Also make sure to use the smallest available package to minimize package parasitics.

## ***My Receiver Sometimes Loses Lock and When I Probe the Signal, the Receiver Always Loses Lock***

- A system such as this may be working marginally
- The small extra capacitance from the probe causes the receiver to lose lock
- This type of system is more difficult to troubleshoot as it requires using all other techniques to improve the overall application
- System / clock noise is often the cause and would be a good place to check first



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This is a typical marginally successful system. There may not be enough signal swing at the receiver inputs or there may be too much noise in the system. Checking the schematic, bypass capacitance, and supply noise would be a good start.

## ***The Receiver Loses Lock Intermittently but Stays Locked If I Change the Cable Length***

- This is one of the most common examples of crosstalk
- This problem can also be caused by reflections
- Sometimes the type of interconnect needs to be changed and this is a cheaper solution than spinning a board layout
- To resolve this problem, signal integrity will need to be evaluated at multiple points along the signal path
  - Often there is only a patch to the problem and the patch is very application specific
- Another reason why verifying board layout and routing is very important in the beginning stages of design



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Crosstalk is a very difficult problem to solve. When multiple channels are used, special attention should be placed on routing through connectors. This may end up saving a lot of troubleshooting time and even possibly save an entire design.

## ***When I Hot Plug My Transmitter, It Doesn't Always Work***

- We guarantee hot insertion capabilities only with our receivers
- However, for transceivers, we support hot insertion
  - In these applications the order of pin contact should be: GND – PWR – I/O



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Hot-insertion and hot-pluggable are terms usually associated with receivers only. Not transmitters. We guarantee that our receivers and transceivers are hot-pluggable.



## ***Comparative Study of Stand-alone LVDS Buffers and SerDes with FPGAs***

## ***Benefits of Discrete LVDS***

- **Lower system cost**
  - Reduced FPGA / ASIC I/O
  - Uses economical connectors
- **Standard supply levels**
- **Broadside pinout allows easy PCB routing**
- **High ESD tolerance for better reliability**
- **Reduced dynamic system power**
- **Efficient Translation between I/O levels**
- **Enhanced signal integrity**
  - Outputs optimized for application
  - Added features like selectable pre-emphasis



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Take-away benefits of discrete physical layer LVDS products.

## **Potential Benefits from using a FPGA with LVDS I/O and SerDes**

- Reduce the number of wires on the PCB because all parallel signals to SERDES are internal to the FPGA.
- Reduce the number of components on PCB
  - However, the un-terminated trace length to the connector becomes longer limiting maximum performance
- Potential to reduce power consumption
  - Depends on the application and number of LVDS I/O resources used on the FPGA



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First and foremost, lowering system cost is a good thing. FPGA companies always will have you pay for features, performance, gates, I/O and package. The number of gates goes hand in hand with the I/O available since the latest fabrication technology has made many FPGA layouts pad limited designs. Higher pin-count packages generally don't have the volumes of lower pin-count packages and will also carry a premium price. Most National LVDS high-bandwidth solutions use moderate speed I/Os of less than 2 Gbps. This allows companies to use economical connectors for new designs or upgrade existing designs with our technology. Using I/Os with speeds in excess of 3 Gbps will often necessitate additional layout / connector / cable / etc. constraints which add to the total system cost.

Most discrete LVDS devices use a standard 3.3V supply level. Often LVDS I/O on an FPGA will require a 2.5V supply level. The additional regulation and board space consumed more than offsets the area and power consumed with a 3.3V discrete solution.

The pinout used for discrete LVDS products offers easy routing to all popular connector styles. The ability to cleanly route signals to and from a connector allows the discrete LVDS devices to be placed in close proximity to connectors or other ICs.

Bus LVDS devices often tout ESD performance well in excess of 4 kV. This robust ESD performance enhances the reliability of any system.

FPGAs that do not have true complimentary outputs require attenuation networks to achieve LVDS-like switching levels. This solution requires two LVCMOS FPGA outputs to drive the attenuation network, doubling the internal dynamic power of the FPGA. This also puts additional stress on the board decoupling scheme.

Often FPGAs with LVDS-like outputs require special VCC I/O levels. This may limit the other types of outputs that can be selected on that I/O bank.



## ***Disadvantages to Using FPGA with LVDS I/O and SerDes***

- The FPGA LVDS signal integrity is poor for speeds > 500 Mbps
  - final test and yield becomes an issue for the FPGA that must meet analog performance criteria - cannot afford to suffer yield hit due to I/O analog performance
- Wasteful of LVDS+SerDes resource unless customer can use all of them. For applications that need less than 4 LVDS channels, FPGA LVDS is definitely not suitable
- Limited options of compression ratio
  - 1:4, 1:7, 1:8, 1:10 & 1:20 only
- Difficult to trouble shoot and expensive to replace
  - Imagine replacing an \$8 LVDS chip vs \$300 FPGA if one of the LVDS channel is down!



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Highly integrated analog IP can result in a heavy upfront FPGA cost and may also lead to increased development costs vs off-the-shelf analog solutions. Also by integrating high-speed components, the coupling between analog and digital sections has a better chance to reach levels sufficient to degrade analog performance characteristics. This becomes more of an issue as the digital section is constrained to higher frequency operation and the programmed functionality represents a majority of the available programmable-logic design elements. As a result of the heavy up-front cost for analog IP, it is unlikely additional analog capability will be included in the specification. This makes it more likely digital resources also will be in short supply.

Separation of the digital and analog resources provides a low-cost path for ensuring adequate digital resources and the ability to plan for future analog needs. High-speed analog functionality and I/O encompasses several input/output standards including Low Voltage Differential Signaling (LVDS), Bus LVDS, Low-Voltage Positive Emitter Coupled Logic (LVPECL), Current-Mode Logic (CML) and derivatives.

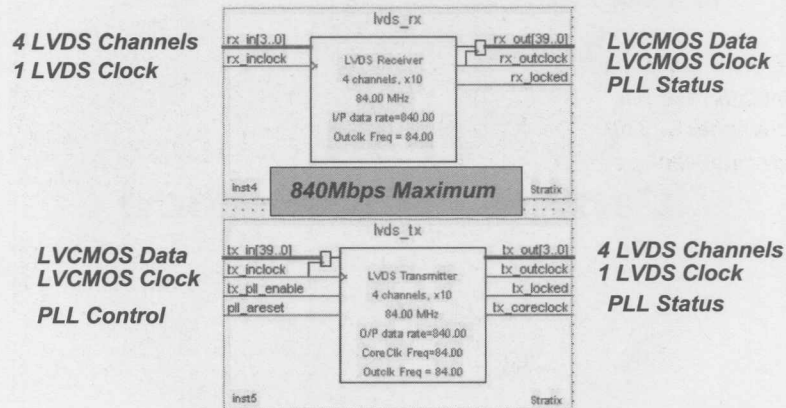
With many of the earlier FPGAs, LVDS performance is limited above 500 Mbps. Before choosing an FPGA for LVDS functionality, a few things the user must consider are the number of channels to use, flexibility, and cost.





## **FPGA SerDes Performance**

## Altera LVDS SerDes I/O Macros



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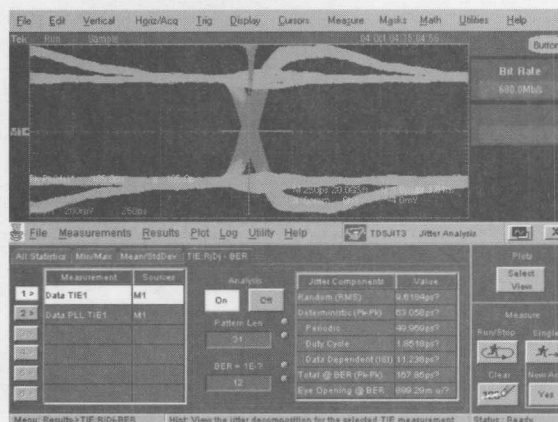


These cells are the basic LVDS I/O building blocks in Altera FPGAs. The overall look and feel is very similar to National's Channel Link SerDes, as we will see later in the presentation.

The cells are configurable for number of LVDS channels, input and output clock divide ratio, control signal use, and status indication. The LVDS I/O on an Altera Stratix device is rated for 840 Mbps, although typical performance can be significantly better than the specification.

## FPGA LVDS SerDes Performance

**Data rate: 600 Mbps**  
**Total jitter: 167 ps**  
**Pre-emphasis: 3 dB**  
**Edge rate: <200 ps**



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Using a Tek 6604 Digital Storage Oscilloscope with a jitter analysis software package, we were able to separate random and deterministic jitter. The total jitter was calculated for a 10-12 bit error rate (BER). Beyond the good overall jitter performance, two additional observations can be made.

The edge rates are symmetric and very fast for sub 1 Gbps performance.

There is 3 dB of built-in pre-emphasis to compensate for backplane or cable loss.

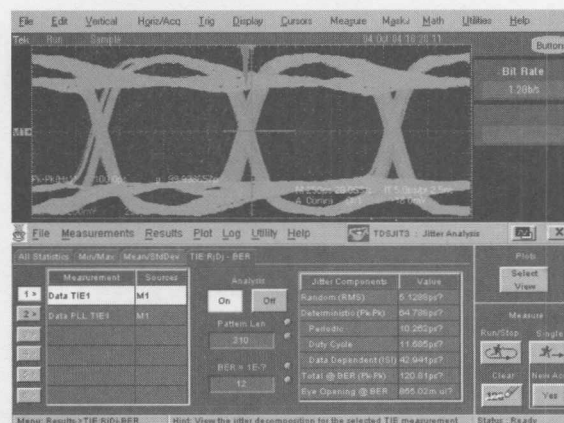
## FPGA LVDS SerDes Performance

**Data rate: 1.2 Gbps**

**Total jitter: 120 ps**

**Pre-Emphasis: 3 dB**

**Edge Rate: <200 ps**



**Typical performance exceeds datasheet specs**



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Due to the performance observed at 600 Mbps, we decided to see how fast the Altera Stratix I/O would continue to operate. As this waveform at 1.2 Gbps shows, significant headroom exists in the 840 Mbps specification. Even adding significant overhead to our serializer implementation on the Stratix FPGA, we consumed only 3% of the overall IC resources, so we don't have a good feel for how much the analog performance would be affected if the FPGA was programmed to handle a large design.

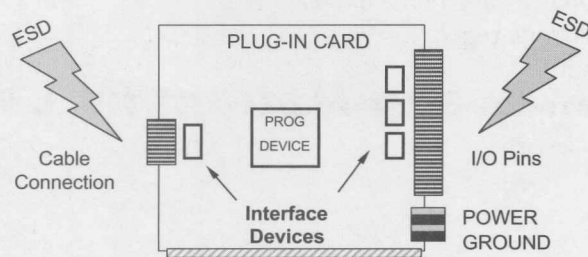
The typical  $F_{MAX}$  performance was approximately 1.5 Gbps.



## **FPGAs and National's LVDS**

## System-Level Issues

### Enhanced ESD protection



Interface Devices have ESD to 12 kV



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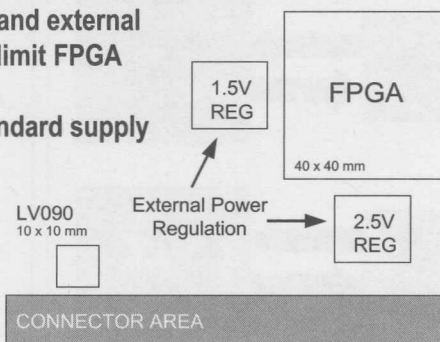


In applications where ESD is of concern, LVDS discrete devices typically are far more robust than FPGAs. Some LVDS discrete devices boast ESD ratings of up to 12 kV (for human body model testing).

For ESD sensitive areas like backplane and cable connections, where it is possible to release a built up static charge, external interface devices are highly recommended. FPGAs and system ASICs are very expensive and can be extremely sensitive to the discharge of static energy. The interface devices can provide an economical means to enhance signal integrity and increase the system resistance to ESD events.

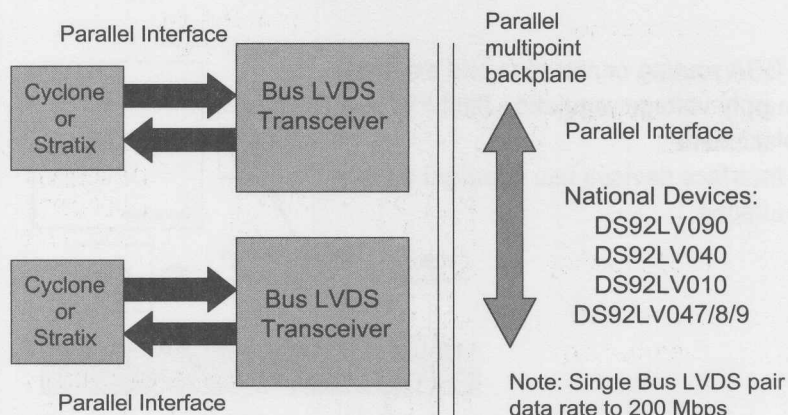
## System-Level Issues

- BGA routing constraints and external supply voltage regulation limit FPGA placement
- Interface devices use standard supply voltages



Due to external supply requirements, it is impossible to place and route a FPGA as close to the connector as a discrete LVDS device.

## FPGA and National LVDS



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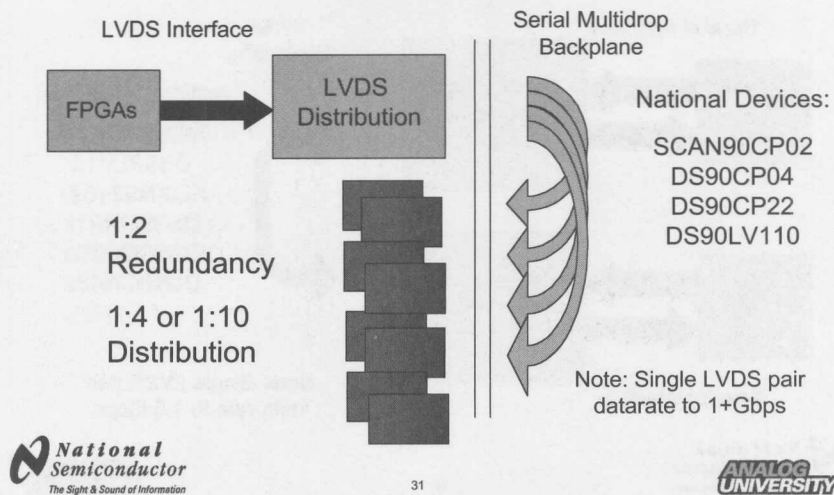
30

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FPGAs that drive multipoint loads over backplanes require noisy high-current LVTTTL drivers to effectively transmit data. The noise to these outputs affects the operation of other noise sensitive FPGA circuits. Translating these signals to Bus LVDS with National transceivers significantly reduces noise on the FPGA and improves routing constraints imposed by the high-current LVTTTL drivers. Since the load is now a single device, low-current, low-noise drivers can be used without paying a speed and system-performance penalty.

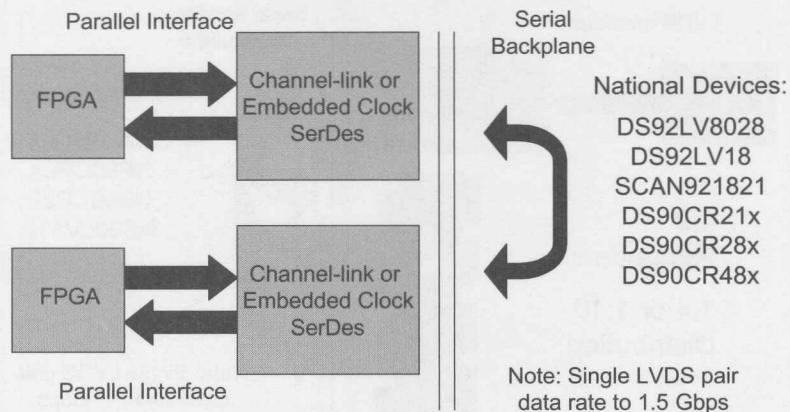


## FPGAs and National LVDS



With the introduction of True-LVDS I/O in some FPGAs, it is possible to drive high-speed LVDS signals across a cable or backplane interface. Creating multiple copies of this signal may constrain FPGA selection or PCB routability. Using a National LVDS switch or data distribution IC can relieve these constraints and result in a more optimal FPGA selection (to reduce cost) and enhanced routing on the PCB.

## FPGAs and NSC LVDS

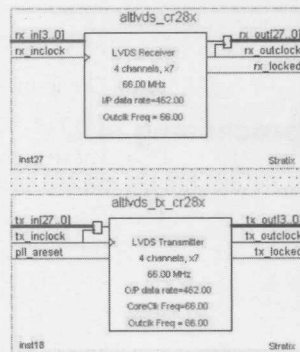


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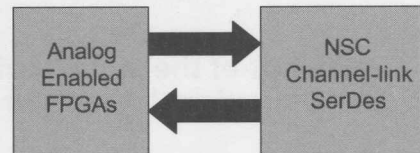


Single National IC bandwidth to 6+ Gbps. Using a digital FPGA for logic programmability and board functionality and National SerDes for board-to-board communications.

## Channel Link Compatibility



LVDS Interface



Note: Direct interoperability with National LVDS devices

Block Diagram  
Analog Enabled FPGAs



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This foil shows how Altera Stratix devices can directly interoperate with National's Channel Link family of SerDes devices.

Xilinx offers a similar function for their Virtex-II line of products.

## ***Life at the Sharp End***

### **The start of the signal-path processing is... the Operational Amplifier**



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Many signal paths start with that most universal of analog components, the operational amplifier\*. First named for its ability to perform mathematical operations (addition, subtraction, integration, differentiation etc) the modern Op-Amp provides the interface to many transducers and sensors, starting the process of converting real-world sensations such as sound, temperature, pressure, and light into electrical signals. Many signal sources simply require amplification or buffering, while others require manipulation to correct transducer or transmission errors. Op-Amps often can combine many of these functions, because the transfer characteristic of an Op-Amp is determined primarily by the external components connected around the Op-Amp.

Despite the fact that the Op-Amp is essentially a five-terminal device, with two input pins, two supply pins (or supply and ground), and one output pin, there are literally hundreds of Op-Amp types. National alone has more than 300 different types of Op-Amp, not counting duals, triples, and quads as separate types, and other manufacturers have similarly large portfolios.

During this seminar we will take a look at the characteristics that distinguish these Op-Amp types, why they are different, and how to choose the "right" Op-Amp. Techniques for solving common Op-Amp problems will be described, along with practical circuit applications.

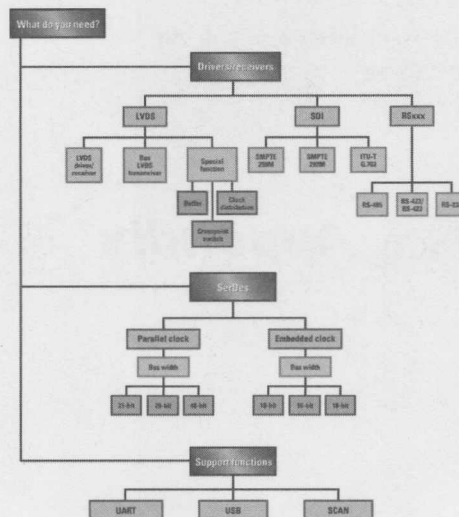
The Op-Amp is only the first part of the signal path. Later on we will show how to accurately convert the signal to a digital format and then transfer that digital data, again without errors, to a storage or processing medium.

However, that is not where the signal path ends. Very often the signal information needs to be put back into a way that we in the "real world" can comprehend, either directly from the source or from the storage medium. Closing the circle, Op-Amps or their cousins are used to drive speakers, display devices, motors and RF transmitters.

\* A notable exception is RF receivers.

## **Appendix**

# Interface Product Tree



2

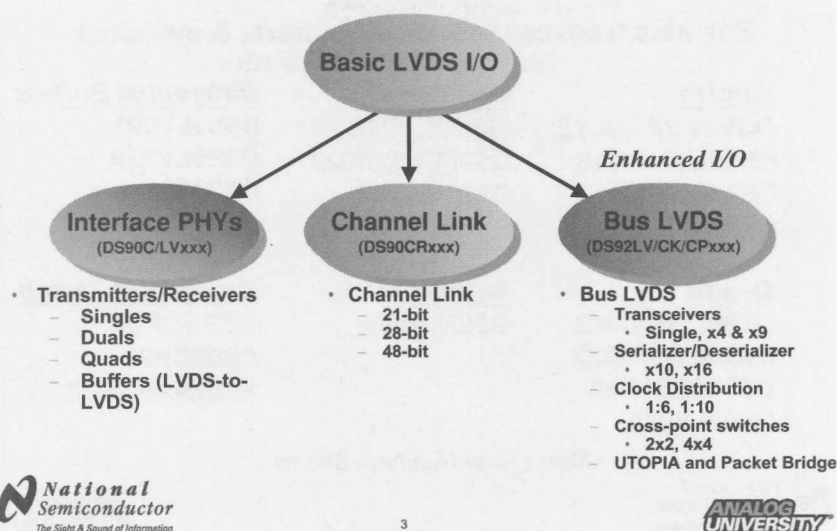


National Semiconductor provides complete interface solutions to empower you to differentiate your products and accelerate time-to-market. Our expertise in high-speed, mixed signal circuits, LVDS technology, and serial standards ensures you will receive the silicon, collateral, and evaluation hardware you need to deliver and create the best products on time at competitive prices.

For all of our interface product lines you will find a wealth of design and application information on our Web site, [lvds.national.com](http://lvds.national.com).

National Semiconductor's interface portfolio of devices is very broad and large. Please see your local distributor or field sales representative for more information on any of these product families.

## National's LVDS Family Tree



Here we have the broad breakdown of National's different types of LVDS products. PHYs are the basic point-to-point transmitters and receivers. In addition, multi-drop applications are allowed. These are good when you only have a few channels of data to transmit or when your data is already serialized.

Channel Link can transmit wide TTL buses, while serializing the data for you. These can be great space and money savers by reducing interconnect costs and complexity. This transmission is done transparent to the designer over just a few differential LVDS lines.

Bus LVDS is an extension of the LVDS line drivers and receivers family, specifically designed for where the bus is terminated at both ends. This family provides a higher current drive so that the effective impedance can be lower than 100 Ohms.

In addition to these three main product lines, there are other enhanced I/O products such as crosspoint switches and very high-speed CML transceivers in the LVDS product line. These specialty products have many useful applications.

## **LVDS Drivers & Receivers**

### **Product Portfolio Examples (not complete list)**

See also transceivers, clock buffers, & switches

Indicates newest products

<u>Singles</u>	<u>Doubles</u>	<u>Differential Buffers</u>
DS90LV011/012	DS90LV049	DS90LV001
DS90LV017/018	DS90LV027/028	DS90LV110
DS90LV019	DS90C401/2	DS92001
DS92LV010	DS36C200	
<u>Quads</u>	<u>9-Channel</u>	<u>Crosspoint Switch</u>
DS90LV047/048	DS92LV090	DS90CP04
DS90LV031/032		DS90CP22
DS90C031/032		SCAN90CP02
DS92LV040		

Note - Root Numbers Shown



4



National drove the standardization and adoption of LVDS and has one of the broadest portfolios of PHY devices.

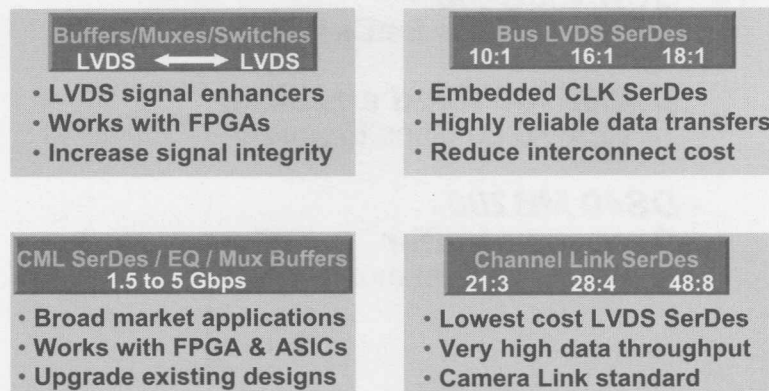
Simple PHYs are available in different channel widths – 1-, 2-, 4-, and 9-channel options are available. For wider buses, multiple devices may be used in parallel depending upon timing margins and bus speed.

As an alternative for wide bus applications, many times a Ser/Des solution is better for point-to-point links due to its smaller interconnect benefits and fewer pins required.

Most devices are 3.3V, but a few are offered for 5V applications. Of course 3.3V and 5V parts can be mixed and matched since LVDS levels are common to both.



## **High-Speed Interface Product Portfolio Families**



5



The high-speed interface products fit into 4 product groupings or families. We group the products by the basic chip functions. These groupings help you understand the benefits that determine why customers choose our LVDS products.

The buffers/muxes/switches family is products that have LVDS as the inputs and the outputs from the devices. This is different than simpler and slower LVDS products that typically translate the LVTTTL I/O on one side of the chip into LVDS signals on the other side. The LVDS-to-LVDS I/O frees these products from the low-speed LVTTTL, and provides the signal integrity features necessary for data-transmission performance. For example, the features are pre-emphasis and equalization. Another good example of the switch application is signaling redundancy.

The next family is the CML (Current Mode Logic) SerDes/EQ/mux buffers. CML is better than LVDS for driving transmission lines at >2.5 Gbps and also works good for rates as low as 1.25 Gbps. This product family is seeing many new additions with products that fit into many applications. For example, there is the recently introduced EQ50F100 equalizer.

Both these families are especially useful for using with the increasing LVDS I/O on FPGAs to increase performance and reliability. Since FPGA LVDS I/O is not the quality necessary for driving transmission lines, customers are using these buffers and switches to ensure the reliability and performance of their data transmission interfaces. TI, Maxim, and Fairchild (FCS) have all copied National's original 2x2 LVDS switch. Both TI and Maxim have been developing newer products with this functionality.

The Bus LVDS SerDes and Channel Link SerDes are families that deliver the serialization functions in 2 different ways. The Bus LVDS SerDes have the clock embedded in the serial data stream and the Channel Link SerDes have an LVDS clock in parallel with the serialized data.

## **National Solutions for High-Speed Backplanes**

- **SCAN50C400**  
– Quad 5 Gbps SerDes
- **EQ50F100 fixed equalizer**  
– 1.25 – 6.25 Gbps Equalizer
- **DS40 MB200**  
**Dual mux-buffer**  
– 1- 4 Gbps dual mux-buffer



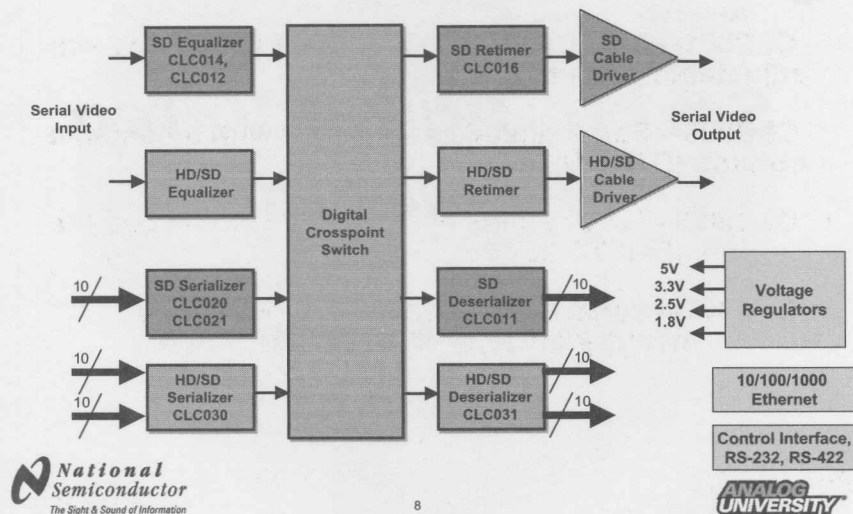


## ***Serial Digital Video Products***

***Megabits @ Many Meters***

National Semiconductor supports the broadcast video industry with a family of products designed to implement the SMPTE 259m and 292m Serial Digital Interface standards. National brings a strong manufacturing tradition to the high performance realm of SDI to make low-cost, high-performance products.

## Serial Digital Video Products



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Routing switchers are the hearts of a broadcast studio. Key features include:

- Categorized by port count
  - Small (16x16 or less), Large (>32x32)
- System implementation
  - Modular design
  - Large frame(s), expandable to 2048x2048
  - Single chassis (up to 128x128)
  - Passive backplane, granularity based on matrix card (32x32 or 64x64)
  - One-rack unit box (<16x16)
- Single format vs mixed format (SD & HD)
  - Modular systems allow both SD and HD I/O cards

## ***SDV Cable Drivers***

- **CLC001—3.3V CMOS serial digital cable driver with adjustable outputs**
- **CLC005—Serial digital cable driver with adjustable outputs (ITU-T G.703)**
- **CLC006—Serial digital cable driver with adjustable outputs (SMPTE 259M)**
- **CLC007—Serial digital cable driver with dual complementary outputs**



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National offers four cable drivers – the latest of these is the CLC001, which operates off of a 3.3V supply rail and has two adjustable voltage outputs.

## ***SDV Receiver Components***

- **CLC012—Adaptive cable equalizer for high-speed data recovery - G.825 LOS**
- **CLC014—Adaptive cable equalizer for high-speed data recovery**
- **CLC016—Data retiming PLL with automatic rate selection**
- **CLC011 Serial digital decoder**



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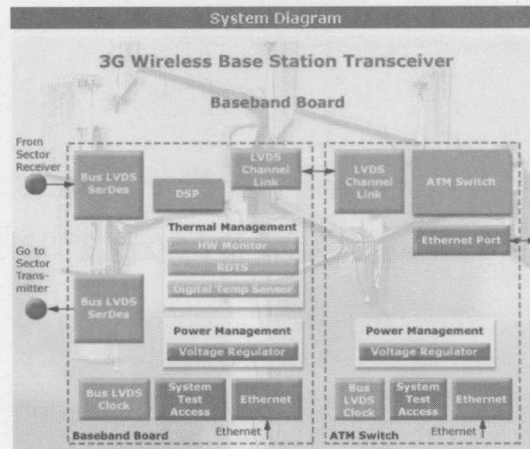
National offers several devices to implement a SDV receiver for standard-definition video.



## **Products for BTS Applications**

The next section displays products used in Base Transceiver Station (BTS) networks.

## 3G Baseband



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The baseband board functionality of a wireless basestation transceiver includes:

- 1) Separating received signals into channels by combining correct time slots or coded messages.
- 2) Sending these signals to the basestation controller for compression.
- 3) Changing to another channel when directed by the BSC.
- 4) Converting channels back into analog, combining multiple voice channels, up-converting to IF, filtering, and amplifying signals for transmission to mobile subscribers.

### Component Highlights

- Buck switching regulators - provide high-efficiency, high-power density power conversion.
- Ethernet PHY - small size, low power, fully interoperable Ethernet PHY delivers up to 1 Gbps performance.
- LVDS - SerDes, ChannelLink, and clock provide high-speed interface between blocks.
- Select from several hardware monitors, RDTs 2-wire serial temperature sensors and SPI/Microwire compatible digital sensors.





## **Low Voltage Differential Signaling & Testability**

SCAN Products

## **What is JTAG?**

- **Joint Test Action Group (JTAG)**
  - Original group working on the standard in 1980's
  - Commonly-used name, but not really accurate
- **IEEE Std 1149.1 Test Access Port and Boundary-Scan Architecture**
  - Official name of this test standard
  - Often just called 1149.1 or just "Dot 1"
- **SCAN**
  - Family name for National's 1149.1 "JTAG" devices
- **SCAN, JTAG, and IEEE 1149.1 names are often used interchangeably**

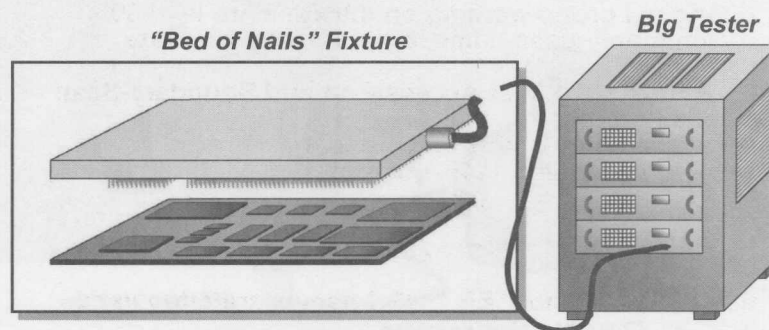


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JTAG is actually an old and inappropriate name for the standard IEEE 1149.1. The technology should really be referred to as IEEE 1149.1 or boundary scan, but since the term "JTAG" is well known by almost everyone in the electronics industry, the word "JTAG" will be used to refer to IEEE 1149.1 technology in the rest of this presentation.

## Before JTAG



- **Test Headaches**
  - An in-circuit "bed of nails" tester (ICT) was used
  - Buried nodes and hidden balls makes this impractical
  - High cost, long development time, and proprietary hardware

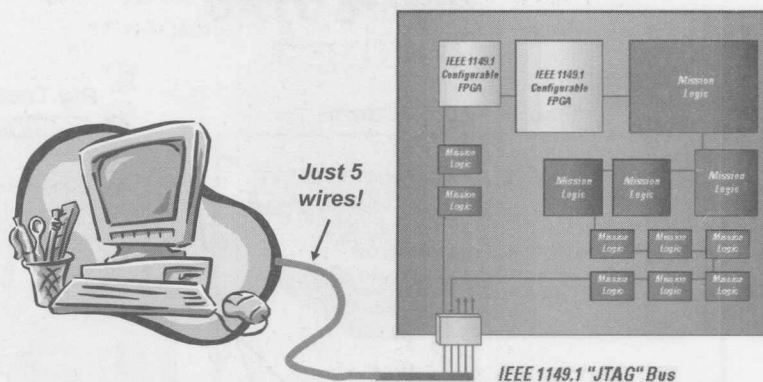
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The old method of testing complex boards involved an in-circuit tester that was expensive, proprietary, and required a long development time. Today's very high density boards, many-layer printed circuit boards (PCBs) with buried nodes, and ball grid array (BGA) packages with hidden balls make such testing very difficult.

## After JTAG



- **JTAG to the rescue**

- Test points are "built into" chips & PC becomes a full test system!!!
- Low cost, short development time, and universal hardware



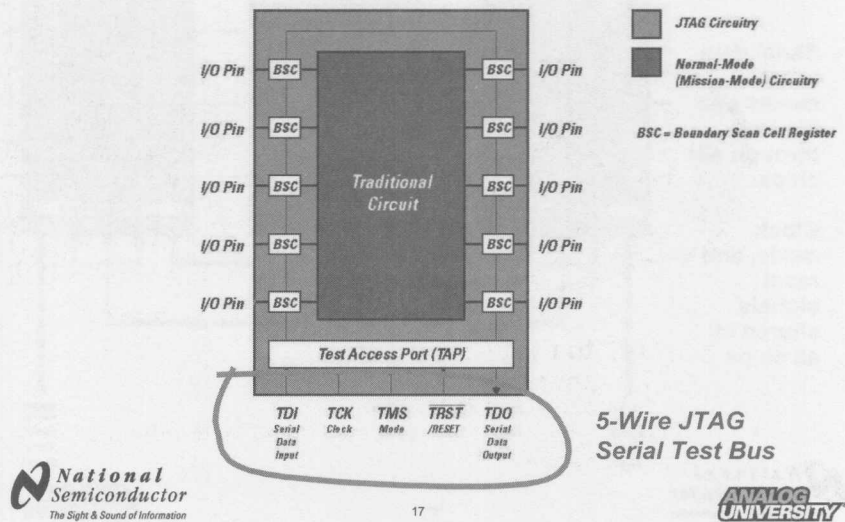
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JTAG technology means test points for each device pin are built into chips and these test points are connected to a 5-wire serial bus. Test development and execution can then be done on a simple personal computer.

## JTAG Is Added "Around" IC

Allows Access to Pins & Internal Nodes



The 5-wire serial JTAG bus (actually, the /TRST pin is optional) consists of:

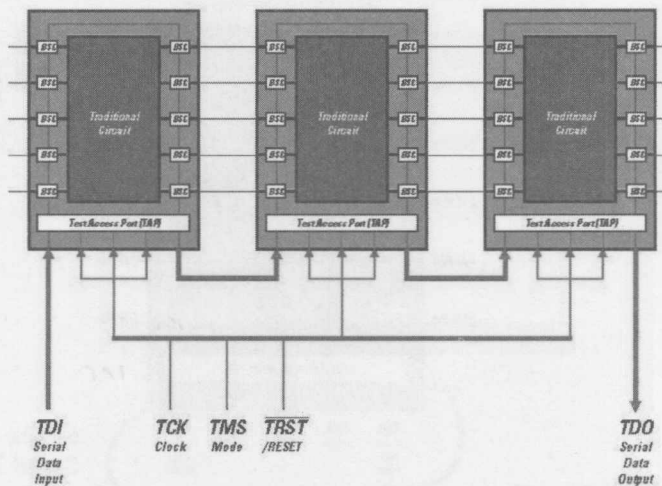
TDI	Test Serial Data Input
TCK	Test Clock
TMS	Test Mode Signal
/TRST	Test /Reset Signal
TDO	Test Serial Data Output

and provides access to the JTAG circuitry in the chip.

## The "SCAN Chain"

### How JTAG is Connected on the PC Board

- Serial data in/out makes one big loop through all chips
- Clock, mode, and reset signals shared by all chips



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The TCLK, TMS, and TRST pins are connected in parallel:

All chips are driven by one TMS signal from the PC  
 All chips are driven by one TCLK signal from the PC  
 (although usually clock buffers are used to drive so many loads)  
 All chips are driven by one TRST signal from the PC

The TDI and TDO signals are daisy-chained together:

PC → Chip 1 TDI  
 Chip 1 TDO → Chip 2 TDI  
 Chip 2 TDO → Chip 3 TDI  
 Chip 3 TDO → Chip 4 TDI  
 Chip n-1 TDO → Chip n TDI  
 Chip n TDO → PC

## **JTAG-Enablers**

**Products Expand Role of JTAG in System Test**

Serializer	Description	Availability
SCANSTA101	Embedded 1194.1 JTAG Test Master	NOW
SCANSTA111	Multidrop Addressable 1149.1 with <u>3</u> JTAG Ports (alias "Bridge")	NOW
SCANSTA112	Multidrop Addressable 1149.1 with <u>7</u> JTAG Ports	NOW

- *These products help customers perform sophisticated JTAG tests in their systems*
- *Have no normal "mission mode" function—JTAG circuitry only inside*
- *Open a range of new, exciting uses for JTAG*



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National provides not only standard chips with JTAG added, but also chips that function only to facilitate sophisticated JTAG operations.

## **Products With JTAG**

### **Buffers with JTAG Support**

Serializer	Description	Availability
SCAN92LV090	9-Channel Bus LVDS Transceiver	NOW
SCAN16512 †	16-bit Universal Buffer	NOW
SCAN16602 †	16-bit Universal Bus Transceiver	NOW

† Bus hold & 25\_ options available.

- **World's first Bus LVDS buffer with JTAG**
  - **Based on National's proven JTAG and Bus LVDS technology**
- **Low-cost universal buffer LVTTTL logic devices**
  - **YES, we sell logic!**
  - **LCX/LVC electricals**
  - **Telecom-friendly 8 x 8 mm 64FBGA (vs. TSSOP)**



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National Semiconductor provides a growing portfolio of products with JTAG. Many new products contain both JTAG and something called at-speed BIST.



## **Products w/JTAG & At-Speed BIST**

### **LVDS Serializers/Deserializers**

- **World's largest selection of 10:1/1:10-bit serializers & deserializers**

- **World's only 10-bit SerDes devices with JTAG & At-Speed BIST**

- **Proven National Bus LVDS performance**

- **Industrial temperature range**

Serializer	Number Channels	Frequency (MHz)	Availability
SCAN921023	1	20 – 66	NOW
SCAN921025	1	30 – 80	NOW
SCAN928028	8	25 – 66	NOW

Deserializer	Number Channels	Frequency (MHz)	Availability
SCAN921224	1	20 – 66	NOW
SCAN921226	1	30 – 80	NOW
SCAN921260	6	20 – 66	NOW
SCAN926260	6	16 – 66	NOW



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National Semiconductor offers a large and growing portfolio of the only Bus LVDS serializers and deserializers with JTAG and at-speed BIST.

## Life at the Sharp End

The start of the signal-path processing is...  
the Operational Amplifier

N/A  
new



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Many signal paths start with that most universal of analog components, the operational amplifier\*. First named for its ability to perform mathematical operations (addition, subtraction, integration, differentiation etc) the modern Op-Amp provides the interface to many transducers and sensors, starting the process of converting real-world sensations such as sound, temperature, pressure, and light into electrical signals. Many signal sources simply require amplification or buffering, while others require manipulation to correct transducer or transmission errors. Op-Amps often can combine many of these functions, because the transfer characteristic of an Op-Amp is determined primarily by the external components connected around the Op-Amp.

Despite the fact that the Op-Amp is essentially a five-terminal device, with two input pins, two supply pins (or supply and ground), and one output pin, there are literally hundreds of Op-Amp types. National alone has more than 300 different types of Op-Amp, not counting duals, triples, and quads as separate types, and other manufacturers have similarly large portfolios.

During this seminar we will take a look at the characteristics that distinguish these Op-Amp types, why they are different, and how to choose the "right" Op-Amp. Techniques for solving common Op-Amp problems will be described, along with practical circuit applications.

The Op-Amp is only the first part of the signal path. Later on we will show how to accurately convert the signal to a digital format and then transfer that digital data, again without errors, to a storage or processing medium.

However, that is not where the signal path ends. Very often the signal information needs to be put back into a way that we in the "real world" can comprehend, either directly from the source or from the storage medium. Closing the circle, Op-Amps or their cousins are used to drive speakers, display devices, motors and RF transmitters.

\* A notable exception is RF receivers.

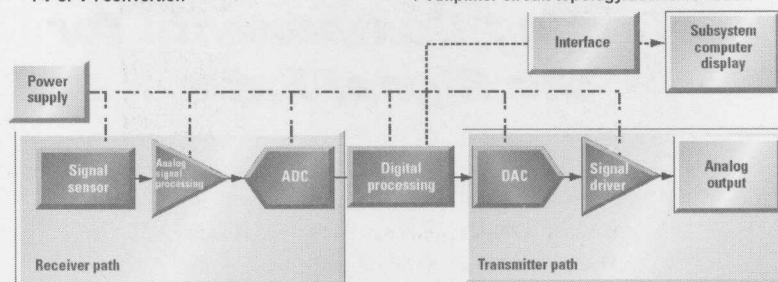
## **Appendix B: Selecting Components for the Signal Path**

1

# A Walk Through the Signal Path (Amplifiers in the Signal Path)

## Basic Features:

- Dynamic Range Adjust
  - Single-ended to Differential
  - Impedance matching
  - Reducing the effects of capacitive loading
  - Remove unwanted signal components
  - I-V or V-I conversion
- Level shifting/ Amplification/AGC
  - signal immunity
  - Signal integrity/SNR
  - Buffer/Driver
  - Filters
  - Amplifier circuit topology/device selection



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When designing a high-speed mixed-signal system, it is good engineering practice to evaluate the block-level signal fidelity through the entire chain step by step. This issue of *Signal Path Designer* focuses on the design of an input or receiver path. The transmitter or output path will be discussed in a future issue. A typical receiver or measurement system is composed of a signal sensor, analog signal processing block, data converter, and digital processing block. Only the analog and mixed-signal portions of the design will be addressed here. Each signal-path block must be carefully selected to achieve desired results.

When op amps are used in signal changes they are often needed to buffer or invert an input signal, gain and amplify it, shift a level and adjust to the subsequent input needs. Furthermore they are used to convert one electrical form into the other: V-to-I (transconductance amplifier) or I-to-V (transimpedance amplifier). Filter functions are often done by operational amplifiers.

Basic features are often to adjust the dynamic range from one output to the other input stage, converting a signal from single-ended to differential transmission form and vice versa, to match impedance or convert impedance to minimize losses and to handle capacitive loading effects (stability). Removing unwanted signal components from the input signal, and providing only the bandwidth of interest to the ADC followed.

**Impedance matching:** Signal sources are not necessarily low impedance. The input of an ADC may well load the source, affecting it. A unity-gain op amp buffer has very high input impedance, and therefore will not load the source. In addition, its low output impedance is well-suited to driving the input of an ADC.

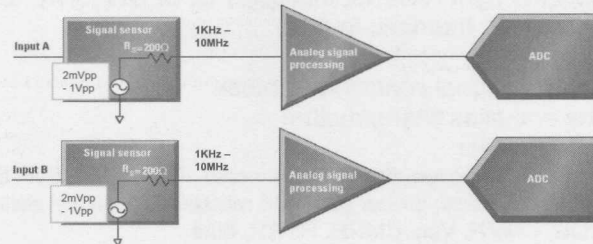
**Reducing the effects of capacitive loading:** Most types of ADCs present a capacitive as well as resistive load on their input. This requires an external compensation circuit, usually a resistor and capacitor. National's datasheets often specifies this network. It is important to

follow the recommendation, but doing so presents a capacitive load to the source. The resistor isolates the source from the capacitor, but is usually a low value. The low output impedance of an op amp interface can usually drive this network with no problem.

**Conversion from single-ended to differential signals:** Even if an op amp is not required for the reasons above, many new analog to digital converters have differential inputs. Most input sources are single ended. Therefore, an op amp interface is required to perform the conversion. This conversion can be accomplished with single-ended op amps, but is more readily accomplished by use of a fully differential op amp.

## Example: Two signal-path receiver system

Typical Application for Medical/Ultrasound or material inspection!



- Dynamic Signal range 54dB
- Minimum SNR requirements: 54dB + 6dB = 60dB
- Theoretical SNR for a 10-bit ADC = 62dB



16-3



System performance requirements must be translated into the specifications of the key signal-path components to achieve the best tradeoffs between performance, power consumption, size, and ease of use. This will walk through a step-by-step design of a typical receiver system that has two signal paths. Each path begins with a sensor operating at frequencies

from 1KHz to 10 MHz and has a single-ended 200ohm output. Sensor signal amplitudes range from 2 mVpp to 1 Vpp and unwanted high-frequency interference is present on both channels. System requirements dictate that minimum signals must be at least 6 dB higher than the system noise for proper signal processing and that maximum signals should not be clipped anywhere in the signal path. As is often the case, power consumption of the design should be minimized.

A possible application for the above signal chain structure could be an medical equipment like and an Ultrasound machine, or an application for none-destructive material testing (reliability test for bridges, check for the steel quality). For certain applications, like TGC (time gain control) measurements, a Variable Gain Amplifier might sit between the transducer/sensor and the single-ended to differential Amplifier (followed by the ADC).

### Selecting the ADC

With the system specifications in hand, designers can begin working on the heart of the input signal path - the analog-to-digital converter (ADC). Key specifications for high-speed ADCs are bits or resolution and sample rate. Since the signal has a dynamic range of 2 mVpp to 1 Vpp or 54 dB and the minimum signal must be at least 6 dB above the noise level of the ADC, the ADC needs a minimum signal-to-noise-ratio (SNR) of 60 dB (54 dB + 6 dB). Theoretically, a 10-bit ADC can have 62 dB SNR, which would meet this requirement. However, 10-bit ADCs don't achieve this theoretical limit. In addition, other components in the chain will contribute noise to the system. Designers will also want to keep the ADC input signal smaller than full scale, which helps eliminate the risk of overdrive. With all of this in mind, a 12-bit converter that can provide 68 to 70 dB SNR is a good choice.

## ***Simplified Design Recipe for an Analog Receive Signal Path***

- First select the right ADC:  $f_s$ ,  $\text{Input}_{\text{BW}}$ , PD, SFDR, SNR, ENOB, Interface to DSP, Interface to Amp
- Design analog signal conditioning block
  - Define anti-alias filter structure
  - Select Amplifier
    - Discuss AC parameter impacts: noise, THD, SNR, BW, Slew
    - DC parameters, proper gain and matching resistors: Swing, VOS, CMVR,  $V_{cc}$ , CMRR, PSRR, bias
- Select anti-alias filter components
- Signal Shift to match ADC Input common mode range



\* Preliminary Information

16-4





## Practical Design Tips for Selecting Signal-Path Products

- ADC resolution vs. Distortion: rule of thumb 6dB per bit:  
 $SNR = 20\log(1/(2^{\text{numbits}}))$ :  
 10 bits = -60dB  
 12 bits = -72dB  
 14 bits = -84dB
- ADC sample rate - Nyquist bandwidth:  $f_{\text{sampling}} = 2f_{\text{signal max}}$   
 → Practical approach  $f_{\text{sampling}} = 10 \times f_{\text{signal max}}$
- ADC typical input 8-10pF || 600Ω



16-5



With the ADC resolution set at 12 bits, sample rate selection is the next step. For an input signal from (close to DC) 1KHz to 10 MHz, a sample rate of at least 20 MSPS is needed from a theoretical point of view. However due to the aliasing effect, some folded spectrum will have not enough attenuation to meet the ADC SNR requirements. Therefore, a four times high samples rate is recommended. In this example, we have chosen an ADC with an 65 MSPS sampling rate, which fulfills as well the requirement for a dual ADC. This allows the full signal frequency range to be digitized by the ADC with no undesired aliasing or folding of signals to frequencies where they might be misinterpreted. This frequency folding or aliasing is discussed in many textbooks and application notes on ADCs and sampling. Looking at the system requirements, there are two other considerations for the ADC. The system has two channels, making a dual ADC beneficial and minimum power consumption desired.

The target ADC specifications are 12-bit resolution, greater than 54 MSPS sample rate, low power consumption, and a dual format. A part that meets these targets is the ADC12DL065, a 12-bit, 65 MSPS, dual ADC with 69 dB SNR and very low (320 mW) power consumption. The ADC12DL065 has other specifications that are important to note as the rest of the signal path is designed. First are the ADC's input characteristics. Its full-scale differential input range is 2 Vpp, common-mode input voltage is 1.5V and input capacitance is 8 pF. Looking at AC specifications for the ADC12DL065, it has excellent SNR and has a spurious-free dynamic range (SFDR) of 76 dB at 30 MHz, ensuring that spurious tones produced by the ADC will be much smaller than desired signals. Another consideration in dual ADCs is the interaction between the two channels; the ADC12DL065 has 80 dB rejection of signals from one ADC input to the other, so that the signals on one channel do not interfere with signals on the other.

## Practical Design Tips for Selecting Signal-Path Products

- Amplifier settling time  $\approx 0.5 * 1/\text{Sampling Freq.}$

### Settling Time:

1MHz:	500ns
5MHz:	100ns
20MHz:	25ns

### Settling Accuracy:

10 bits = 0.1%
12 bits = 0.024%
14 bits = 0.006%

- Amplifier  $SR_{\max} = 2 * \pi * f_{\text{signalmax}} * V_{\text{peak}}$  (slew rate)
- $SNR = 6.02 * n + 1.76\text{dB}$  → Only valid over entire Nyquist BW!
- Correction term:  $SNR = \dots + 10\log(fs/2BW)$  → Oversampling effect!



16-6



• It can be shown, that the ratio of the rms value of a full scale sinewave to the rms value of the quantization noise in an ADC (expressed in dB) is:

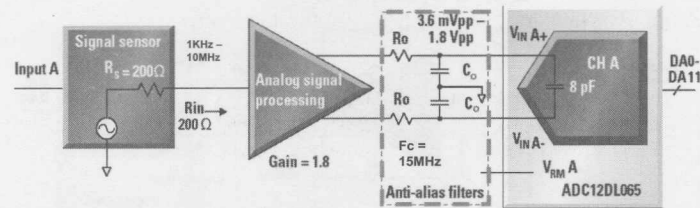
•  $SNR = 6.02 * n + 1.76\text{dB}$ , where n is the number of bits in the ideal ADC. This equation is only valid if the noise is measured over the entire Nyquist bandwidth from DC to  $fs/2$ .

• If the bandwidth is less than  $fs/2$ , then the SNR within the signal bandwidth BW is increased because the amount of quantization noise within the signal bandwidth is smaller. The correct expression for this condition is expanded by the term:  $\dots + 10\log(fs/(2 * BW))$ .

• The equation above reflects the condition called oversampling, where the sampling frequency is higher than twice the signal bandwidth. The correction term is often called 'processing gain'. Note that for a given signal bandwidth, doubling the sampling frequency increases the SNR by 3dB.



## Define Anti-alias Filter



- minimize attenuation
- reduce folding and aliasing effects
- optimise filter characteristic for passband and stopbands

→ Webench for Amplifiers!



16-7



The analog signal conditioning block

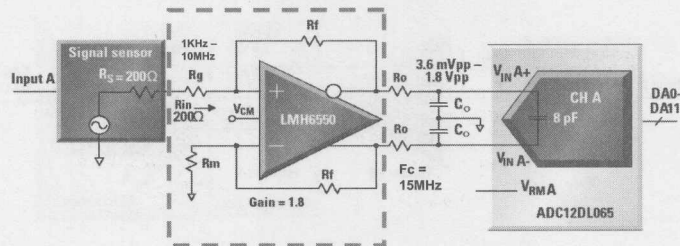
Next the analog signal conditioning block should be designed to enhance the performance of the ADC. Functions in this key block are filtering to remove unwanted high-frequency signals, impedance matching for the sensor outputs, conversion from the sensor's single-ended signals to the ADC's differential signals, amplification to match signal levels to the ADC input range, and level shifting to match the ADC common-mode input level. Select components to minimize the component count in this block. Because there are high-frequency signals that need to be removed and also a need to reduce the bandwidth of the input noise to the ADC, this example design uses a simple, passive, single-pole, low-pass filter between the amplifier and ADC. A 3 dB bandwidth of 15 MHz is chosen for two reasons:

- To minimize attenuation of signals at the upper end of the input signal range
- To reduce the aliasing or folding of noise and unwanted signals from frequencies beyond half of the ADC sample rate into the frequency band of interest.

A filter as specified here is often called an anti-alias filter, since it eliminates or reduces the effect of aliasing. Depending on the amplitude and frequency of the unwanted AC signals, a steeper, multi-pole filter might be required, but for this application the single-pole filter is sufficient. The filter is a simple resistor-capacitor (R-C) filter with values that will be chosen after the design of the amplifier block that precedes the filter.

## Select the Amplifier!

Single-ended to differential conversion!



First order noise calculation:

$$V_{nadc} = V_{namp} * \sqrt{BW} * (1 + \text{Gain}) =$$

$$V_{namp} * \sqrt{15 \text{ MHz}} * 2.8 \leq 125 \mu\text{Vrms}$$

→ SEE AN-104 for details



16-8



The designer's next step is to look at one of the more demanding requirements for the analog signal processing block - the function of single-ended-to-differential conversion. This is often done with transformers, but since the signal frequency range includes DC, the transformer will not work and a single-ended to differential amplifier will be required. This amplifier can also provide amplification, level shifting, and impedance matching functions. The process of converting system specifications to amplifier specifications is similar to the process for selecting the ADC. Key high-speed amplifier specifications are bandwidth, gain, noise, and distortion. To avoid degradation of the signal before it gets to the ADC, an amplifier bandwidth of several times the 10 MHz signal bandwidth is desired. Since the full-scale ADC input is 2 Vpp and the maximum signal is 1 Vpp, an amplifier gain of two would amplify the 1 Vpp maximum signal to exactly match the ADC full scale. To avoid the possibility of the amplified signal overdriving and clipping the signal at the ADC input, the gain will be set slightly lower at 1.8. The SNR of the ADC12DL065 is 69 dB. This means that the total noise of the ADC is 69 dB below the 2 Vpp full scale input level or about 250  $\mu\text{Vrms}$ . The amplifier output noise should be at least a factor of two smaller than this or less than 125  $\mu\text{Vrms}$ . To translate this noise level into the noise voltage and current specifications for the amplifier, the bandwidth of the amplifier output signal and the gain of the amplifier must be taken into account. The previously selected anti-alias filter bandwidth of 15 MHz sets the bandwidth of the amplifier noise presented to the ADC, and the amplifier gain is set at 1.8. ADC input noise due to amplifier input voltage noise is calculated with the following equation:

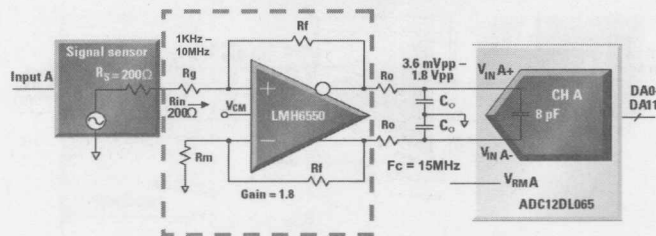
$$V_{nadc} = V_{namp} * \text{rt}(BW) * (1 + \text{Gain}) = V_{namp} * \text{rt}(15 \text{ MHz}) * 2.8 \leq 125 \mu\text{Vrms}$$

So the input noise of the amplifier,  $V_{namp}$ , needs to be less than 12 nV/rtHz. There may also be noise contribution from the input currents of the differential amplifier and that contribution will be checked later when the resistor values around the amplifier have been set. Distortion is not a key specification of this system, but the amplifier distortion should be in the same range as the ADC

distortion. A single amplifier for each channel will be selected to facilitate clean PC board layout and to maximize rejection of high-frequency interference between the two amplifier inputs. The requirement is for a single-ended-to-differential amplifier with a bandwidth greater than 80 MHz at a gain of 1.8, input noise less than 12 nV/rtHz, and distortion terms suppressed by greater than 70 dB. National's new LMH6550 differential, high-speed op amp meets these requirements well. Gain bandwidth product for this amplifier is 400 MHz, so at a gain of 1.8, the bandwidth will be 140 MHz (400 MHz / (1+1.8)). Input voltage noise of the LMH6550 is 6 nV/rtHz, which is better than the 12 nV /rtHz requirement, and the amplifier's distortion for a 20 MHz 2 Vpp signal is typically 70 dB, which is in the same range as the distortion of the ADC.

## Calculate Gain-Setting Resistors!

Impedance mismatching causes code offset in the ADC!



$$R_{in} = R_s = 200\Omega$$

$$R_g = R_{in} / (1 + \text{Gain}) = 200\Omega / (1 + 1.8) = 71.4\Omega$$

$$R_f = \text{Gain} \times (R_g + R_s) = 1.8 \times (71.4\Omega + 200\Omega) = 488.5\Omega$$

$$R_m = R_g + R_s = (71.4\Omega + 200\Omega) = 271.4\Omega$$

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Using a few simple equations, differential operational amplifiers like the LMH6550 can be set to a range of gains and input impedances by properly selecting the external gain and feedback resistors. The desired amplifier gain is 1.8, and the desired input resistance is 200 Ohms. Using the following equations, the resistor values are selected:

$$R_{in} = R_s = 200.$$

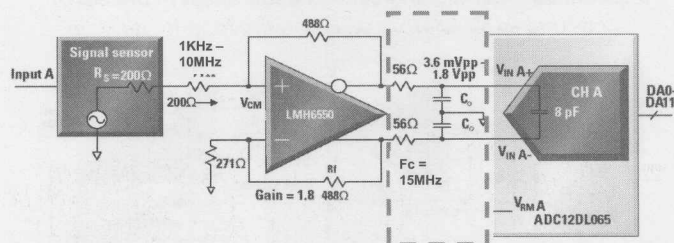
$$R_g = R_{in} / (1 + \text{Gain}) = 200. / (1 + 1.8) = 71.4.$$

$$R_f = \text{Gain} \times (R_g + R_s) = 1.8 \times (71.4. + 200.) = 488.5.$$

$$R_m = R_g + R_s = (71.4. + 200.) = 271.4.$$

A quick check of the amplifier input-noise current contribution with these resistance values reveals that the amplifier noise is dominated by the voltage noise term that was previously calculated, so the contribution from input-noise current will be ignored.

## Calculate Anti-aliasing Filter Components



$$F_c = 1 / (2\pi * R_o * (C_o + C_{adc} * 2))$$

$R_o$  resistor value chosen between  $47\Omega$  to  $100\Omega$

$$C_o = 1 / (2\pi * R_o * F_c) - C_{adc} * 2 =$$

$$1 / (2\pi * 56\Omega * 15 \text{ MHz}) - 8 \text{ pF} * 2 = 173 \text{ pF}$$



16-10



The values for the resistors and capacitors in the anti-alias filter can be selected now that the amplifier characteristics are known. The desired cutoff frequency for the filter is 15 MHz; the equation for the cutoff frequency is:

$$F_c = 1 / (2\pi * R_o * (C_o + C_{adc} * 2))$$

The LMH6550 datasheet includes an example of an anti-alias filter with a 50 MHz cutoff frequency, and the suggested  $R_o$  is 56. This  $R_o$  value will be used in this design and  $C_o$  will be adjusted for the 15 MHz cutoff frequency.

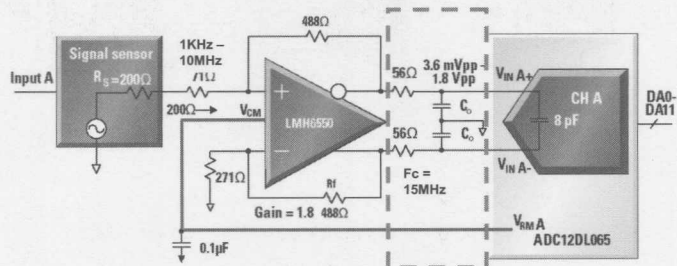
$$C_o = 1 / (2\pi * R_o * F_c) - C_{adc} * 2 =$$

$$1 / (2\pi * 56\text{ohm} * 15 \text{ MHz}) - 8 \text{ pF} * 2 = 173 \text{ pF}$$

All of these resistor and capacitor values can be adjusted to allow for more commonly available values. All of these resistor and capacitor values can be adjusted to allow for more commonly available values.

## Signal Shift to Match ADC Input CMVR

Internal ADC reference close's the loop to set  $V_{cm}$ !



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One final function is required of the amplifier – signal shifting to match the common-mode input of the ADC. Common-mode voltage adjustment is accomplished simply in the LMH6550 by applying the desired common-mode voltage, 1.5V from the ADC12DL065 reference output pin, to the amplifier  $V_{cm}$  input. The resulting amplifier output common-mode voltage will be 1.5V and will match the ADC input common-mode voltage.



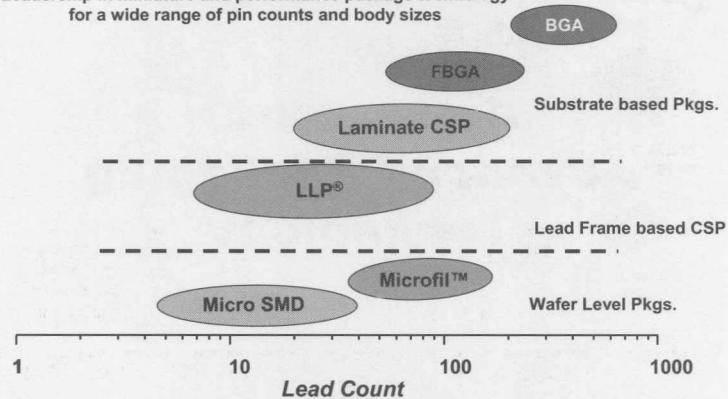


## **Appendix C: Advanced Packaging Technology**



## Advanced Package Families

Leadership in miniature and performance package technology  
for a wide range of pin counts and body sizes



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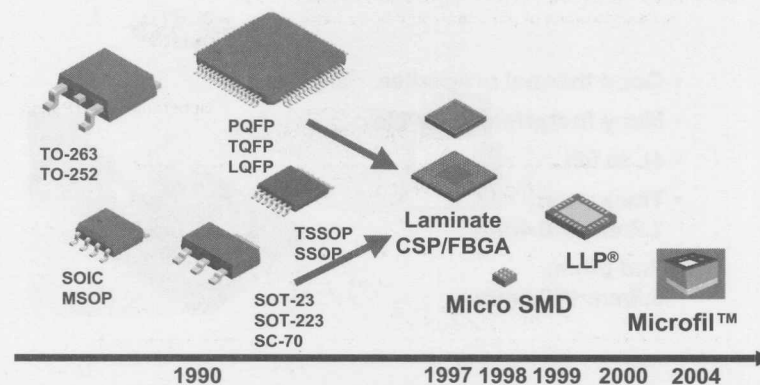
17-2

**ANALOG UNIVERSITY**

- Extremely wide range of body size and pin count package portfolio....miniature packages to complex and high performance BGAs
- Packages are categorized into wafer level, lead frame, and substrate based.



## Miniature Package Introductions



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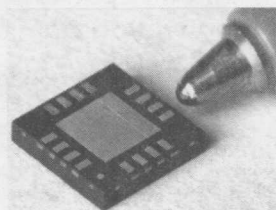
17-3

**ANALOG**  
UNIVERSITY™

- Package miniaturization (performance improvement) is one of the key driving factors driving growth for Analog products
- We are the trend setters in introducing
  - micro SMD and Microfil (wafer level package)
  - LLP (Lead-frame based CSP)

## ***Leadless Leadframe Package, LLP®***

- Good thermal properties
- Many footprints possible
- 4L to 56L
- Thickness:  
1.2mm→0.4mm
- Pad pitch:  
0.5mm→0.4mm



17-4

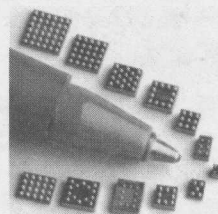


The LLP is a low thermal resistance package that is readily configured for many different footprints.

Heat is coupled efficiently to the PCB, which then has the burden of spreading the heat.

## ***micro SMD***

- Industry's smallest, thinnest package innovation from National
- Smaller die, lower lead count products up to 42L
- Pad pitch:  
0.5mm → 0.4mm



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**Web Page**  
**<http://www.national.com/packaging/>**

**Package Information**

**Plastic Packages**

- Selection Guide by Package Type
- Introduction to LLP (Leadless Leadframe Package)

**Hermetic Packages**

- Selection Guide by Package Type

**Application Notes**

- Leadless Leadframe Package (LLP)
- Micro SMD
- Bumped Die Package
- Laminate CSP
- Ball Grid Array
- Microfit™

**Package Initiatives**

**Lead-Free Status**

- For ordering information please contact your local National Semiconductor sales representative.
- Questions & Answers
- European Directive Compliance
- What's driving the move to lead-free solder processes?
- National's Lead-free Strategies
- Industry Consortia
- Lead-Free 260° C Reflow Profile
- Literature

**General Packaging Information**

- LLP Footprints in GERBER Format
- Package ID cross-reference table
- Device Marking Conventions
- Process Recommendations
- Package Reliability
- Advanced Packaging Technology
- Plastic
- Hermetic
- Manufacturing Considerations
- Other Packaging Information
- Solder Information



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